Synopsys' New Designware USB 2.0 nanoPHY IP to Cut Power and Size in Half

Enables Longer Battery Life and Lower Cost for Mobile and High-Volume Consumer Products

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the addition of the new DesignWare® USB 2.0 nanoPHY IP to its existing DesignWare USB 2.0 physical layer (PHY) product line. The new mixed-signal PHY IP builds on Synopsys' three years of leadership in successfully providing USB 2.0 PHY intellectual property (IP) in more than two dozen process node and configuration combinations. The new DesignWare USB 2.0 nanoPHY IP is tailored specifically for low-power consumption, small area, and high yield. It targets designers of mobile, high-volume consumer applications such as next generation handheld game machines, feature-rich smart phones, digital cameras, and portable audio and video players.

Over the last three to four years, designers have successfully integrated the USB 2.0 bus interface into many systems-on-chip (SoC) designs. The initial applications started with PCs and then moved into peripherals such as printers, scanners, and external hard drives that were typically plugged into a power source. However, as the bus standard has become more pervasive, it has been quickly adopted into a wide range of battery powered consumer applications that are more cost sensitive and require very low power.

"This new DesignWare USB 2.0 nanoPHY IP follows many years of success with our volume-proven USB PHY IP solution," said Guri Stark, vice president of Marketing, Solutions Group at Synopsys. "Our experience with leading semiconductor companies has enabled us to continuously innovate and address our customer's needs for low-power, cost-competitive IP that helps deliver high yield, reduced area and increased interoperability. As part of our complete USB IP solution, we expect the new PHY IP to be adopted in many cost- and power-sensitive designs for the competitive mobile and consumer market."

Availability

The new DesignWare USB 2.0 USB nanoPHY IP is expected to be available starting in Q1 of calendar 2006.

About DesignWare Mixed-Signal IP (MSIP)

Synopsys' comprehensive portfolio of high-performance mixed-signal PHY IP for the PCI Express®, SATA, XAUI and USB protocols, as well as a suite of I/O libraries, enables designers to quickly integrate high-performance interfaces into their next-generation systems-on-chips (SoCs). Available for industry-leading processes, the DesignWare MSIP portfolio meets the needs of today's high-performance SoC designs for the networking, storage, computing, and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controllers and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually, on a fee-per-project basis, or users can opt for the Volume Purchase Agreement, which enables them to license all the MSIP in one simple agreement. For more information on DesignWare MSIP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations for adoption of the USB 2.0 USB nanoPHY IP and the expected date of availability the USB 2.0 USB nanoPHY IP. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of (i) unforeseen difficulties in completing development of the commercial release of the USB 2.0 USB nanoPHY IP, (ii) lower-than-expected customer demand for the USB 2.0 USB nanoPHY IP, (iii) uncertainties attendant to any new product release and (iv) certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2005

entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations -- Factors That May Affect Future Results."

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