Synopsys Announces Source-Code License for SystemVerilog Verification Library

VMM Standard Library Enables Adoption of Techniques in the ARM-Synopsys Verification Methodology Manual (VMM) for SystemVerilog

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the availability of the SystemVerilog source code for its implementation of the VMM Standard Library, a base-class library to accelerate the adoption of the SystemVerilog standard for verification. The VMM Standard Library is specified in the ARM-Synopsys book Verification Methodology Manual for SystemVerilog, announced by Springer Science + Business Media, Inc. today. The library enables users to adopt the advanced verification techniques and methodology advocated in the book more quickly and easily.

"By making their implementation of the VMM Standard Library available as source code, Synopsys is providing a jump-start to designers to use the verification techniques contained within the VMM for SystemVerilog," said Tim Holden, director, EDA relations, ARM. "This will enable our Partners to apply sophisticated SystemVerilog verification methodologies to their ARM® technology-based designs and will benefit other SoC designers in the electronics industry as a whole by offering a way of standardizing verification."

Synopsys' VCS® comprehensive RTL verification solution includes the object code for the VMM Standard Library. VCS customers may license the source code at no additional cost to gain insight into the implementation details. SystemVerilog Catalyst Program members may also license the VMM Standard Library source code at no additional cost to facilitate compatible methodology support for their EDA tools, verification IP and services. SystemVerilog Catalyst Program members can provide compiled, object-code versions of the library to their customers. Synopsys' implementation of the VMM Standard Library is based on IEEE P1800 SystemVerilog for easy tool interoperability, and has been extensively tested with the VCS solution.

"Making source-code to Synopsys' implementation of the VMM Standard Library available is a big step toward driving wide adoption of SystemVerilog," said Michael Garcia, design and verification methodology manager at Freescale Semiconductor. "This will enable a high degree of EDA tool interoperability, particularly with the advanced capabilities of SystemVerilog, thereby improving verification productivity and helping to achieve first-silicon success with even the most challenging chips."

"Synopsys has been on the leading edge of SystemVerilog from the very beginning, when our donations accelerated the development of the language's verification features," said Rich Goldman, vice president, Strategic Market Development at Synopsys. "We continue that leadership by co-authoring the VMM for SystemVerilog book with ARM and by making our implementation of the VMM Standard Library freely available to the industry."

Availability

VMM Standard Library object code is available today for VCS users. VMM Standard Library source code, which can be used with EDA tools compliant with IEEE P1800 SystemVerilog, is planned to be available for license at no additional charge by VCS users and SystemVerilog Catalyst members before the end of the year.

Synopsys Discovery Verification Platform

The Discovery™ Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera® and Synopsys' proven Reference Verification Methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About the SystemVerilog Catalyst Program

Synopsys' SystemVerilog Catalyst Program promotes the development and use of EDA tools, verification IP and training services supporting the SystemVerilog standard for design and verification. Corporate members of the SystemVerilog Catalyst Program may gain access to Synopsys' design and verification tools including: VCS, HDL Compiler™, the front-end language compiler for Design Complier®, and Leda® for the purposes of developing SystemVerilog-based tools, ensuring their

interoperability and providing support for mutual customers.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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