# NVIDIA Adopts Synopsys' Design Compiler Topographical Technology

Cites Predictability, Faster Time-to Market and Ease of Deployment as Key Benefits

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NVIDIA Corporation, a worldwide leader in programmable graphics processor technologies, is deploying the "topographical technology" in Synopsys' Design Compiler® Ultra to increase the competitiveness and accelerate time-to-market for its next-generation designs. The ability to accurately predict key characteristics of a design, such as timing and area, during the early stages of development allows NVIDIA's designers to synthesize a better netlist for physical implementation. This results in significant productivity gains, fewer design iterations, and faster time-to-market.

"We believe Design Compiler's topographical technology is a better approach to synthesis, generating results that more closely correlate to physical implementation and therefore reduce iterations between synthesis and physical tools," said Dan Smith, director of hardware engineering at NVIDIA. "The topographical technology fits readily into our design flow, delivering area and timing correlation which is within three to six percent of post- placement results. In addition, with this technology we are realizing reduced congestion. These results, complemented by the improvements we have seen in DC Ultra 2005.09, are driving our decision to deploy this technology on our next-generation designs."

The topographical technology in Design Compiler utilizes Synopsys' advanced placement and optimization algorithms to bring accurate timing and area context into the synthesis engine, eliminating synthesis dependency on wireload models. This results in very close timing and area correlation between synthesis and physical design, giving RTL designers early visibility into downstream design issues and eliminating costly iterations between synthesis and layout.

"The topographical technology extends Design Compiler's capabilities well beyond timing, area, power, and test optimization, making the RTL-to-GDSII design flow more predictable than ever before," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Market leaders like NVIDIA recognize that this technology is an essential component in meeting their aggressive design goals and schedules."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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