Synopsys and TSMC to Optimize RTL-to-Wafer Design Process

Companies Expand Strategic Design Collaboration to Bridge Design and Manufacturing Interdependencies

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) (NYSE: TSM), the world's largest dedicated semiconductor foundry, today announced a new collaborative, holistic approach to integrating semiconductor design and manufacturing. This optimized approach aligns design tools, mask creation, fabrication and test to achieve common goals for final silicon. The new initiative is dedicated to increasing cost effectiveness of 90 nanometer (nm) designs and below, and to reducing time to market by focusing on design for manufacturing (DFM) issues such as improved yields, low power consumption and higher performance.

TSMC brings its portfolio of leading-edge process technologies and process-proven libraries to the collaboration while Synopsys contributes its industry-standard design platforms and DFM family of products. Leveraging the key strengths of each company, the expanded commitment and combined resources will be dedicated to the development of technology solutions and design platforms that can meet the challenges of semiconductor design beyond the 90-nm node.

"This expanded collaboration will benefit designs at and beyond the 90 nanometer node," said FC Tseng, deputy chief executive officer, TSMC. "As leaders within our respective industries, TSMC and Synopsys are focused on accounting for all aspects of the final design through the entire design process, rather than relying on a sequential set of tasks performed in isolation. By working together, we can influence what improvements are needed for process libraries, implementation tools and DFM processes to provide designers with optimized solutions."

"Synopsys and TSMC continue to strengthen our already productive relationship by collaborating on all critical steps in the design development process -- from RTL to wafer. By tying our entire set of design and DFM solutions directly to the process, designers can achieve better yields on parts, while meeting power and performance requirements in fewer design iterations," said Aart de Geus, chairman and chief executive officer of Synopsys. "We have identified the key issues that directly impact customer designs at 90 nanometers: low power, high performance and time-to-yield. These seemingly incompatible demands are specifically targeted and addressed through our collaboration with TSMC."

Dr. de Geus will serve as keynote at the TSMC Symposium, which will take place today at the San Jose Convention Center.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates one advanced 300mm wafer fab, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly-owned subsidiary, WaferTech, and its joint venture fab, SSMC. In early 2001, TSMC became the first IC manufacturer to announce a 90-nm technology alignment program with its customers. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see http://www.tsmc.com/ .

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: Synopsys is a registered trademark of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: editorial, Dan Holden of TSMC, +1-408-382-7921, or dholden@tsmc.com; or Eileen Hunt of Synopsys, Inc., +1-650-584-5374, or elhunt@synopsys.com; or Julie Crabill of Edelman Public Relations, +1-650-429-2732, or Julie.crabill@edelman.com, for Synopsys, Inc.

Web site: http://www.tsmc.com/

Web site: https://www.synopsys.com/