StarGen Verifies Advanced Serial Switched Interconnect Chips With Synopsys' VCS, VERA and VCS Verification Library Solutions

Project Methodology Leverages Assertions, Functional Coverage, Constrained-Random Stimulus Generation and PCI Express® Verification IP

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that StarGen, the innovation leader in advanced interconnect semiconductors, has successfully verified two large, complex switching chips using Synopsys' VCS® comprehensive RTL verification, Vera® testbench automation and VCS Verification Library solutions from the Discovery™ Verification Platform. These chips use the StarGen AXSys architecture for performance, flexibility, reliability and scalability, leveraging both the Advanced Switching Interconnect (ASI) and PCI Express® standards for connectivity. AXSys is an ideal board- and system-level interconnect solution for system OEMS in the compute, storage and communications sectors.

"We found the combination of the VCS and Vera solutions to be extremely powerful in verifying our Merlin Switch and Kestrel PCI Express-ASI Bridge chips," said Ernie Grella, director of Chip Development at StarGen. "Vera's parallel constraint solver, with its high performance and ability to solve constraints over arrays, was essential for setting up efficient and effective chip-level testbenches. We used both assertions and functional coverage within the Vera tool to enhance our verification environment. We are currently migrating our environment to the VCS Native Testbench (NTB) technology to achieve even greater performance."

The StarGen engineering team used Vera-based testbenches for standalone verification of major blocks as well as for full-chip verification. StarGen's methodology took advantage of DesignWare® PCI Express verification IP (VIP) from the Synopsys VCS Verification Library to validate conformance to the industry standard interface protocol. The VIP in the VCS Verification Library tightly integrates with the Synopsys Reference Verification Methodology and supports native compilation by VCS NTB for higher performance.

"Verification success requires a combination of technologies, linked by a comprehensive methodology," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "Constrained-random stimulus generation, coverage-driven verification, assertions and verification IP each play a part in ensuring that chips can be taped out on time with first-silicon success."

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®, and Synopsys' proven Reference Verification Methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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