Synopsys and Altera Collaborate to Deliver ASIC-Strength Flow Supporting Altera's Stratix II FPGAs and HardCopy II Structured ASICs

Synopsys' ASIC Compatible Design Flow Including DC FPGA and Formality Products and Professional Services Now Supports Altera's Stratix II and HardCopy II Families

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced support for Altera's HardCopy II structured ASIC and Stratix II FPGA families. Customers can now use the Design Compiler® FPGA (DC FPGA) solution from Synopsys' Galaxy™ Design platform tools and the Formality® functional equivalence checking tool to prototype a design in a Stratix II FPGA and seamlessly migrate to a HardCopy II structured ASIC or standard cell ASIC from one unified front-to-back design flow.

Support for Altera's latest devices extends the collaboration between Synopsys and Altera for accelerating the implementation of Stratix II FPGAs and HardCopy II structured ASICs. The two companies have also developed a new timing-driven back-end design flow, based on the Astro™ solution and tools included in Synopsys' Galaxy Design platform, which optimizes the performance and time-to-results for customer implementations. Using the entire Synopsys flow, including the DesignWare® Library and the PrimeTime® timing solution for prototype and implementation, Synopsys' Professional Services (SPS) group has taped out several first-generation HardCopy designs for Altera's customers and will be one of the first to have HardCopy II structured ASIC capabilities in production. Additionally, SPS supports Altera's HardCopy design center to ensure the final chip implementations adhere to design rules, timing budgets and optimal place and route specifications.

"ASIC designs today are highly complex therefore, designers are reducing risk by using FPGAs to prototype their ASIC. The introduction of Altera's Stratix II FPGA and new HardCopy II structured ASIC provides another alternative to standard cell ASICs," says Alain Bismuth, vice president, HardCopy product group at Altera. "The combination of Synopsys' ASIC-strength design solution, including DC FPGA, Formality, PrimeTime and DesignWare Library, with Altera's industry-leading Stratix II FPGAs and HardCopy II structured ASICs, is the preferred solution for ASIC designers. It provides them the flexibility to prototype in Stratix II FPGA and seamlessly migrate the design to Hardcopy II structured ASIC or re-target to cell based ASIC."

"We have worked closely with Altera, to ensure that our mutual customers get their designs to silicon via a low risk flow that yields the best results in the fastest time," said Gal Hasson, director of marketing, ASIC and FPGA Synthesis at Synopsys. "Designers who use Altera's high-performance FPGAs and structured ASICs know that they can rely on the proven Synopsys tools and services and the ASIC-like flow to meet their performance and time-to-market goals.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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