NVIDIA Adopts Synopsys' Physically Aware Test Solution for Latest Processor Designs

Galaxy 2004 Delivers Higher Test Quality Through Bridging Fault Support in TetraMAX DSMTest

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, announced that NVIDIA Corporation has adopted Synopsys' Galaxy™ 2004 physically aware test solution for its latest generation designs. On large deep sub-micron (DSM) devices -- where increasingly more silicon area is consumed by wires rather than transistors -- there are relatively more manufacturing defects arising from bridging (wire-related) faults than from stuck-at (transistor-oriented) faults. Synopsys' Galaxy 2004 test solution addresses this challenge and allows NVIDIA to use layout extraction information to generate bridging fault tests with TetraMAX® DSMTest.

"We worked closely with Synopsys to improve modeling of DSM defects when we realized this would become a key test requirement for our upcoming graphics processor designs," said Dan Smith, director of hardware engineering at NVIDIA. "Synopsys now provides us with complete automatic test pattern generation support for bridging faults. Using TetraMAX DSMTest enables us to test for transition, bridging and path-delay faults, and thereby improve the quality we deliver to our customers."

To meet their corporate quality and cost mandates, designers need a test automation solution that delivers the highest fault coverage with fastest time-to-results without impacting the overall design flow. Synopsys' Galaxy Test addresses these challenges with a unified test automation solution for RTL-to-manufacturing test. By supporting bridging fault extraction with Galaxy's Star-RCXT™, TetraMAX DSMTest provides a fully automated bridging fault solution. DFT Compiler™ SoCBIST further minimizes the cost of testing for all TetraMAX fault models, including bridging faults.

"Synopsys has worked closely with NVIDIA to understand and address its key test requirements, and we are excited with our combined results," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Our support for bridging fault models in TetraMAX DSMTest further demonstrates our strategy to deliver the most advanced test capabilities to our customers."

Galaxy Test is a complete test automation solution for RTL-to- manufacturing test. This unified solution -- anchored by Synopsys' DFT Compiler, SoCBIST, and TetraMAX ATPG products -- eliminates costly iterations between design synthesis and test implementation and enables IC designers to achieve timing, area, power and DFT closure simultaneously.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

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