Synopsys Unveils New Breed of DFM Products to Solve Process-Related Variation Issues at 45nm and Beyond

Innovative Process-Aware DFM Product Family Enables Designers to Reduce Process Variability Impact and Improve Design for Advanced Semiconductor Manufacturing

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today unveiled a new family of process-aware design-for-manufacturing (PA-DFM) products that analyze variability effects at the custom/analog design stage for 45-nanometer (nm) and smaller designs. As feature sizes continue to shrink, variability arising from advanced silicon technologies, such as strain engineering, increasingly affects circuit performance. The PA-DFM product family's core products -- Synopsys Seismos and Paramos -- link manufacturing variation information back to design, enabling custom IC (IP, cell, memory and analog) designers to optimize layouts and maximize yields. This product family is another key element in Synopsys' drive to help customers improve yields at every critical point throughout the design-to-manufacturing process.

The PA-DFM product family is uniquely equipped to account for transistor variability, a critical capability in the DFM space. These products address the parametric variations that arise from design and manufacturing interactions by integrating accurate physical modeling information in the design process. Building on Synopsys' TCAD expertise in advanced process and device modeling, these latest additions to the Synopsys DFM offering complement the company's recently announced PrimeYield suite of yield-analysis tools as well as its PrimeTime® VX statistical timing analysis and Star-RCXT™ VX statistical extraction tools.

Ken Liou, director of the IP and Design Support Division at UMC, said, "Process variability presents more and more DFM challenges for designers as new process steps are added for advanced technology nodes. For example, current modeling solutions cannot yet account for how contact placement will impact the stress film that may be used to enhance mobility. We are happy to see the development of these new DFM Solutions for 45 nanometer and beyond."

To help ensure seamless integration with the existing design infrastructure, the PA-DFM products are built to easily "drop in" to customers' existing custom design flow and methodology, protecting their investment while fulfilling a critical need for reduced variability and increased circuit performance. The PA-DFM products allow custom IC designers to realize the full potential of technology scaling and, in turn, expand the latitude for yield maximization.

By integrating TCAD-derived models with physical design tools, Synopsys is uniquely positioned to fill a critical void in the design flow of nanometer ICs. Together with the company's industry-standard HSPICE® circuit simulation tool and PrimeTime® VX and Star-RCXT™ VX tools, the PA-DFM product family underscores Synopsys' focus on optimizing variation awareness for increased performance, productivity and predictability. All of these tools are highly complementary, enabling customers to cover their bases with respect to variability issues from cell layout through design implementation.

Family Includes Powerful Set of Capabilities

Together, Seismos and Paramos address two major sources of variability in a design: proximity variations due to stress and other neighborhood effects, and global variations due to the spread of manufacturing process parameters across different die and wafers. By utilizing accurate physical models of the manufacturing process, custom designers can account for manufacturing variability without major changes to the current physical design flow.

Seismos is a transistor-level tool for the analysis of stress and other proximity effects in nanometer strained-silicon technologies. As the 65nm technology node ramps to volume production and the 45nm technology node enters pre-production, customers need the capability to analyze parametric variations caused by proximity effects, such as the impact of layout on transistor stress state. Seismos is the first EDA tool to address this critical need. Its models are based on rigorous TCAD simulations validated by silicon data. The tool can easily handle multimillion-transistor designs.

Paramos links SPICE models directly to manufacturing conditions by extracting process-aware SPICE compact models that combine calibrated TCAD simulations with global SPICE extraction. It allows customers to simulate the impact of process variability (statistical or systematic) on circuit performance. This methodology provides customers with a physically based variation model for statistical timing simulations of circuit performance, allowing them to explore designs' sensitivity to real physical process parameters.

"At 45 nanometers and below, our customers must understand both the impact of variation and the sources of this variation. Synopsys' new process-aware DFM product family provides our customers with increased understanding of the underlying

physical phenomena that cause process variations," said Wolfgang Fichtner, general manager of the Synopsys TCAD business unit. "In addition, the tools allow our customers to take full advantage of Synopsys' TCAD, DFM and variation-aware statistical analysis technologies to explore and optimize their process and design methodologies, further closing the loop with silicon. This can lead to significant time and cost savings and, ultimately, to higher yield for chip makers."

The PA-DFM product family is available now.

About Synopsys TCAD

Technology computer-aided design (TCAD) refers to the use of computer simulation to model semiconductor processing and device operation. TCAD provides insight into the fundamental physical phenomena that ultimately impact performance and yield. The PA-DFM solution leverages Synopsys' expert knowledge in TCAD modeling, advanced process and device engineering, design and EDA to link manufacturing variation information back to design with accurate physical models.

About Synopsys DFM

With its design for manufacturing (DFM) tools, Synopsys is expanding on what is already the industry's most comprehensive DFM solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, PrimeYield LCC, PrimeYield CMP and PrimeYield CAA technologies, Hercules™ physical verification tool, Proteus OPC, CATS® mask data preparation product, SiVL® lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chip (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys has its headquarters in Mountain View, Calif., and has offices in more than 60 locations throughout North America, Europe, and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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