Synopsys Unveils Latest Innovation in RTL Synthesis, Eliminating Wireload Models

Design Compiler® 2005 Delivers Accurate Correlation to Post-Layout Timing for RTL Designers

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today introduced the latest innovation in RTL synthesis by announcing Design Compiler® 2005 release, eliminating synthesis dependency on wireload models. The Design Compiler 2005 solution includes a new, innovative "topographical technology" that enables designers to accurately predict post layout timing and area during RTL synthesis without the need for wireload model-based timing approximation. Created for RTL designers, the Design Compiler 2005 release requires no physical design expertise or changes to the synthesis use model. By accurately predicting post-layout timing, this solution eliminates costly iterations between synthesis and layout, providing faster time to results. Design Compiler 2005 is part of Synopsys' Galaxy™ Design Platform.

"Timing convergence on our challenging designs often requires costly iterations between RTL synthesis and physical design," said Jeff Lukanc, director of Engineering for the IDT™ (Integrated Device Technology, Inc.) serial-switching division. "We are impressed with the results from the new topographical technology in the Design Compiler 2005. Without requiring wireload models, timing results were within four percent of post layout timing, which represents a 9x improvement in correlation. Area was within one percent of post layout, representing a 6x improvement in correlation. We look forward to deploying this innovative technology from Synopsys which will significantly reduce costly iterations and accelerate our time to results."

"Accurate timing information in synthesis can significantly improve the productivity of our RTL designers as well as our customers," said Keith Clarke, vice president of Engineering, ARM. "With the Design Compiler 2005 release, we have seen a 4x improvement in timing and area correlation between synthesis and layout on the ARM1136JF-S™ processor without having to use wireload models or change the recommended synthesis flow."

The topographical technology in the Design Compiler 2005 solution brings accurate net delay estimation into RTL synthesis without requiring any physical expertise from the user. It utilizes Synopsys' best-in-class placement and optimization technologies to drive accurate timing prediction within the synthesis engine, ensuring significantly better correlation to the final physical design. The Design Compiler 2005 solution increases RTL designers' productivity by enabling them to focus on real design issues in the synthesis phase and create a better starting point for physical implementation. Sharing this technology between the Design Compiler product and the Galaxy physical design solution reduces time-consuming iterations and improves time to results by driving a convergent RTL to GDSII flow.

"The design methodology at SGI is based heavily on physical information and real physical floorplan information is difficult to procure early enough to drive synthesis," said Eric Fischer, physical design manager at SGI. "This is where the new topographical technology in Design Compiler 2005 brings potentially great value to our design teams. Accurate timing prediction during synthesis enables our RTL designers to improve the design while still in the synthesis phase, generate a better starting point for layout and accelerate timing closure. We are encouraged to see that Design Compiler 2005's timing prediction was within 1 percent of post layout timing without requiring any physical information. Design Compiler 2005 is proving itself to be extremely valuable. We are eager to integrate it into our design methodology."

"Designers today need to produce highly competitive products within very short schedules. They rely on the comprehensive synthesis capabilities of Design Compiler software to meet their timing, area, power and test goals within the shortest possible time," said Antun Domic, senior vice president and general manager, Implementation Group, Synopsys. "Now, with the new topographical technology in the Design Compiler 2005 release, designers can accurately predict post-layout timing without the use of wireload models or the need for physical expertise. Once again, Synopsys is changing the state of the art in RTL synthesis by delivering higher designer productivity and faster time to results."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at: https://www.synopsys.com/ .

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CONTACT: Heather Kettmann of Synopsys, Inc., +1-650-584-4723, or kettmann@synopsys.com; or Sarah Seifert of Edelman, +1-650-429-2776, or sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/