Synopsys Introduces 'MinChip' Technology Delivering Smallest Possible Chip Size for Volume Applications

Synopsys JupiterXT and IC Compiler Tools Enable Die Size Optimization

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today introduced new MinChip technology that analyzes physical design complexity and identifies the smallest routable size for semiconductor designs. The technology is integrated into the physical design flow in Synopsys' JupiterXT™ floorplanning tool and IC Compiler place-and-route solution. MinChip technology automates the process of identifying the smallest routable area for a design. Optimal results are achieved in hours, saving weeks of manual effort while taking into account all potential area savings. The new Die Size Optimization methodology enabled by MinChip delivers critical value for high-volume applications where even small area savings has a significant impact on overall cost per chip.

Synopsys Die Size Optimization methodology delivers the smallest possible chip size at tapeout. Following optimization by IC Compiler, MinChip technology is applied to the design. In hours, it returns a result that represents the minimum area in which the design can be implemented and remain routable while retaining the characteristics of the original floorplan. The resulting design is then taken through the normal design closure process. MinChip utilizes Synopsys' best-in-class placement and routing technologies to drive accurate routing prediction, ensuring correlation to the final physical design. This new capability automates a task that otherwise requires complex scripts and countless implementation runs to reach the same result. For high volume applications, modest area savings can represent a significant yield improvement. In internal testing at Synopsys using customer taped out designs, average area reductions of 9% were observed.

"The benefit of being able to implement a design at the smallest chip size for high-volume applications is clear," said Antun Domic, senior vice president and general manager, Implementation Group, Synopsys. "Die size optimization enabled by JupiterXT and IC Compiler allows designers to incorporate an area-optimization step into their tapeout schedule with minimal effort and the possibility of huge payback because of the reduced area. Once again, Synopsys is raising the bar by delivering higher designer productivity at the lowest possible cost per chip."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

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Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com

Web site: https://www.synopsys.com/