Genesis Microchip Adopts Synopsys' DFT MAX Adaptive Scan

DFT MAX Achieves 90% Test Data Volume Reduction for Flat Display TV Controller

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Genesis Microchip Inc., a leading supplier of display image ICs, has successfully deployed DFT MAX to reduce tester costs. DFT MAX's Adaptive Scan technology enables scan compression that reduces both test application time and test data volume by up to 50x over traditional scan techniques. Genesis designers achieved 90 percent test data volume reduction on a recent design for a flat panel display controller which led to their decision to adopt DFT MAX within the Galaxy(TX) Design Platform solution.

"We have seen measurable test cost reduction with Synopsys' DFT MAX -- from RTL synthesis through physical implementation -- and are very satisfied," said T. Chan, senior vice president of product development, Genesis Microchip. "DFT MAX's Adaptive Scan technology is a straightforward extension to traditional scan currently being implemented at Genesis using Synopsys' DFT Compiler, Physical Compiler® and TetraMAX® ATPG design flows. Tester time reduction, along with low area impact on the design, are the main driving forces leading to our adoption of DFT MAX."

Packaging requirements limited the number of pins available for testing Genesis' controller IC. These limitations could have led to a substantial increase in the amount of test data required per pin along with an increase in tester costs associated with managing the larger data volume. Genesis designers used DFT MAX with the Galaxy™ Design product family to substantially reduce the number of test patterns, thereby meeting both their packaging constraints and their test coverage needs. To Genesis's satisfaction, when the device was fabricated, the ATPG test patterns passed on the tester within hours.

"There is a growing need to reduce both test data volume and test application time to lower tester costs as well as make room in memory for the additional tests needed to detect deep submicron defects," says Graham Etchells, director of marketing, Synopsys Test Automation Business Unit. "What has been missing in the industry is a solution that is as easy to implement as scan, and works concurrently with downstream physical design flows. With DFT MAX we have achieved that goal and, given all the successes our customers are having with it, we believe DFT MAX will become the de facto standard for scan compression."

DFT MAX Adaptive Scan utilizes advanced scan compression technology to minimize tester costs by reducing both test application time and test data volume by up to 50x compared with traditional scan techniques. DFT MAX's key advantage is that it is easy to implement and is less intrusive on design flows and design performance than alternative methods. Fragmented bolt-on flows requiring separate design synthesis and test compression insertion steps can break critical timing, add routing congestion and necessitate subsequent re-optimization. DFT MAX by contrast is integrated with the Galaxy physical design flow to eliminate costly, time-consuming design iterations between synthesis and physical implementation. Simultaneously, designers achieve convergence of timing, power, area and test.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the rate of adoption of Synopsys' DFT MAX product. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of difficulties in predicting future customer demand and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2005 entitled "Factors That May Affect Future Results."

NOTE: Synopsys, Physical Compiler, and TetraMAX are registered trademarks of Synopsys, Inc. Galaxy is a trademark of Synopsys. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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