Synopsys Expands Access to Advanced Chip Design Capabilities Through European Chips Design Platform

Supporting the European Chips Act, startups and research teams will gain access to Synopsys chip design solutions to advance Europe's strategic goals in areas such as AI and high-performance computing (HPC)

Highlights

- Simplified access to Synopsys' advanced EDA design software through the EuroCDP
- Support covers both Level 1 and Level 2 of the EuroCDP program, from the earliest-stage ventures through pre-production
- Broad EDA coverage includes full digital front-end and back-end flows for advanced AI and HPC SoC designs on leading-edge process technologies, as well as photonic integrated circuit (PIC) and analog/mixed-signal (AMS) design flows

BRUSSELS, Nov. 4, 2026 – Today at The Technology Sovereignty Package in Practice event in Brussels, Synopsys, Inc. (Nasdaq: SNPS) announced an agreement with the European Chips Joint Undertaking (Chips JU) to make its electronic design automation (EDA) software available to semiconductor startups and medium-sized enterprises (SMEs) through the European Chips Design Platform (EuroCDP).

Synopsys' agreement with EuroCDP will provide a new, simplified entry point for advanced chip innovation by giving semiconductor designers streamlined access to Synopsys' leading design tools, in addition to EuroCDP's full program offering IP, training, funding and prototyping support.

"Europe's next generation of semiconductor innovation will come from organizations of many different sizes, not only established chip companies. EuroCDP is designed to give startups, SMEs and research teams a clearer pathway to the resources they need to develop new technologies. Expanding the platform with Synopsys' advanced design capabilities is an important part of making Europe's chip innovation ecosystem more accessible and dynamic." said Jari Kinaret, Executive Director of the Chips Joint Undertaking, Chips JU.

Supporting European Innovators at Every Stage
Synopsys will support both Level 1 and Level 2 of the EuroCDP program, so participants can use Synopsys solutions from the earliest stage of their venture through pre-production. By providing full digital front-end and back-end flows, including advanced SoC design on leading-edge process technologies at key foundries, Synopsys is supporting Europe's strategic goals in areas such as AI and high-performance computing (HPC). Synopsys also supports photonic integrated circuit (PIC) flows for optical networking, data centers, and sensing, and analog/mixed-signal (AMS) flows for industrial, automotive, and connectivity applications.

EuroCDP members will gain access to the same Synopsys production-proven design, verification and signoff solutions deployed by leading semiconductor companies worldwide to accelerate their innovation.

"Europe has a strong foundation of world-class semiconductor research and entrepreneurial talent. EuroCDP can help build on that strength by expanding access to the advanced design capabilities innovators need to turn ideas into silicon," said Antonio Varas, Chief Strategy Officer, Synopsys. "By joining the initiative, Synopsys is helping EuroCDP members accelerate their design process, contributing to the goals of the European Chips Act and a stronger, more competitive European semiconductor ecosystem."

A Long-Standing Partner to European Innovation
Through its work with emerging semiconductor companies across Europe, including Axelera AI, Openchip and SiPearl, Synopsys has developed deep experience helping innovators around the world to tackle advanced SoC design. EuroCDP provides an opportunity to bring that experience to the next generation of European semiconductor companies.

Axelera AI leveraged a range of Synopsys digital design and implementation and verification technologies in the development of its Metis and Europa AI Processing Units (AIPUs). These capabilities were complemented by advanced power-integrity technology from Ansys, now part of Synopsys, helping Axelera AI optimise power delivery, performance and energy efficiency.

"Europe has the technical talent and innovation potential to build a world-leading semiconductor ecosystem, but giving emerging companies access to advanced design technologies and expertise is critical to turning that potential into successful products. Synopsys and EuroCDP can help lower those barriers, enabling more startups and research teams to develop their capabilities, accelerate innovation and expand semiconductor design expertise across Europe," said Giuseppe Garcea,

Director of Strategic Procurement & Founding Team Member, Axelera AI.

Synopsys at the European Industrial Alliance on Semiconductors
The annual event in Brussels will bring together senior representatives of the European Commission, the Chips Joint Undertaking, EuroCDP, executives from leading EDA and IP providers and European semiconductor companies, as well as a broad audience of industry representatives and experts.

During the event, Antonio Varas, Chief Strategy Officer at Synopsys will take part in a panel on “Accelerating Chip Design in Europe”, moderated by Pierre Chastanet, Head of Microelectronics & Photonics, European Commission.

Resources

- Learn more about EuroCDP: eurocdp.eu
- Learn more about Synopsys EDA solutions: www.synopsys.com

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

Forward-Looking Statements
This press release contains forward-looking statements, which involve risks, uncertainties and other factors that could cause Synopsys’ actual results, time frames or achievements to differ materially from those expressed or implied in such forward-looking statements. Information on potential risks, uncertainties and other factors that could affect our results is included in filings we make with the SEC from time to time, including in the sections entitled “Risk Factors” in our latest Annual Report on Form 10-K and in our latest Quarterly Report on Form 10-Q. Synopsys undertakes no duty, and does not intend, to update any forward-looking statement provided in this press release, whether as a result of new information, future events or otherwise, unless required by law.

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