Synopsys Showcases Comprehensive Autonomous Engineering Workflows from Silicon to Systems, Developed with NVIDIA Technology

New long-running, fully agentic workflows spanning EDA to CAE multiply engineering productivity

Key Highlights

- Synopsys unveils a fully autonomous long-running design verification agent that orchestrates the entire chip verification cycle delivering up to 50X faster time-to-validated RTL while achieving 20% additional coverage improvement
- Demonstrating Synopsys' first fully autonomous computer-aided engineering (CAE) workflow for thermal management and electronic device cooling capable of autonomously executing set-up, pre-processing, and post-processing in a fraction of the time required for manual approaches
- Expanded portfolio of more than 20 GPU-accelerated Synopsys EDA and multiphysics products, including 18X speedup of PrimeSim™ SPICE simulations

SUNNYVALE, Calif., July 26, 2026 /PRNewswire/ -- Today at the 2026 DAC Chips to Systems Conference, Synopsys, Inc. (NASDAQ: SNPS) announced advancements to agentic AI for engineering in collaboration with NVIDIA. Synopsys has developed fully autonomous, long-running agentic capabilities for chip design and electronics system design enabled with NVIDIA Nemotron on NVIDIA's accelerated computing platform and secured by the NVIDIA OpenShell runtime. Demonstrated at DAC for the first time, Synopsys' capabilities promise to be a force multiplier for R&D teams beyond task agents, transforming time-consuming chip verification and thermal simulation into automated insight delivery, engineering productivity, and system performance improvement engines.

"AI is fundamentally reshaping engineering, and Synopsys is at the forefront of this transformation, enabling fully autonomous agents across every stage of silicon and systems development," said Ravi Subramanian, Chief Product Management Officer at Synopsys. "Our close collaboration with NVIDIA continues to accelerate the development of next-generation AI technologies by combining Synopsys' domain expertise spanning EDA and CAE with NVIDIA's advanced AI infrastructure and technologies. Together, we are enabling a new class of autonomous engineering workflows that elevate productivity, unlock deeper insights, and help customers innovate faster."

"The future of engineering is agentic, where AI agents reason, plan, execute complex workflows and verify their own work across the entire product development lifecycle," said Tim Costa, Vice President and General Manager for Computational Engineering at NVIDIA. "Synopsys is using NVIDIA AI tools and accelerated computing to build simulation and AI physics agents that help teams close verification, automate thermal analysis and compress development cycles from weeks to hours."

Introducing Synopsys' Fully Autonomous Design Verification (DV) Workflow
Coverage closure has been among the most significant bottlenecks in the DV process. Despite assistive tools, engineering teams spend significant labor and compute resources on incremental improvements. The companies are evolving the DV approach from tool-assisted to a goal-driven workflow that autonomously pursues coverage closure and traces root failure causes throughout development.

The solution, built on Synopsys' agentic AI platform and powered by Synopsys AgentEngineer™ technology and NVIDIA's agentic AI infrastructure — including NVIDIA Agent Toolkit, NVIDIA Nemotron 3 Ultra open model, and OpenShell runtime — features a fully autonomous, long-running orchestrator agent. The orchestrator agent deconstructs DV goals from specification, design, test repository, and user inputs, and orchestrates specialized agents and tools in a closed loop workflow spanning the full chip verification lifecycle, from test plan generation to coverage closure and advanced debug. Demonstrated at DAC, the end-to-end fully autonomous verification closure agentic flow compresses weeks of manual labor into hours of agentic execution that achieves up to 50X faster time-to-validated RTL with an additional 20% improvement in coverage.[1]

Autonomous Analog & Mixed-Signal (AMS) Workflows
AI-powered Custom Compiler™ Layout Synthesis (CCLS) is laying the foundation for autonomous analog and mixed-signal (AMS) design by automating layout generation, optimization, and design-layout convergence. Building on these capabilities, Synopsys AgentEngineer™ technology orchestrates multi-step analog flow spanning design creation, SPICE simulation, implementation, and verification. Engineers define design intent and performance goals in natural language, while autonomous agents execute and optimize the workflow, accelerating design closure and improving productivity by up to 3X.[2]

Delivering Autonomous Engineering Agents Across Design and Simulation
Synopsys developed a fully autonomous agentic CAE workflow for electronics thermal analysis using NVIDIA Agent Toolkit and

NVIDIA CUDA-X libraries. Built with Ansys Icepak® electronics cooling simulation software — now part of the Synopsys portfolio — and open-source PyAEDT libraries, the agentic workflow autonomously executes simulation set-up, pre- and post-processing in a fraction of the time required for traditional approaches.

Extending the Value of GPU Acceleration to More Engineering Workflows
Synopsys continues to accelerate innovation with the industry's broadest portfolio of more than 20 GPU-enabled EDA and multiphysics products, unlocking deeper analysis and faster time-to-market across the design flow — from physical verification to photonics simulation. Recent developments include:

- PrimeSim™ SPICE circuit simulations perform up to **18X faster** leveraging NVIDIA GPUs.[3]
- Synopsys QuantumATK® accelerates next-generation semiconductor material innovation by up to 50X for Gaussian-basis quantum chemistry simulations enabled by cuEST and up to 200x faster machine-learned force field simulations using NVIDIA Blackwell GPU infrastructure.
- Ansys Lumerical FDTD™ 3D electromagnetic simulation software achieved a **10X speedup** on NVIDIA GPUs compared to CPUs when used within Synopsys' Multiphysics Fusion™ solution for analog and photonic design.
- In addition, Synopsys continues its deep collaboration with NVIDIA leveragingCUDA-X libraries to accelerate its solvers, including cuLitho, cuDSS, cuEST, and use cases in development with the newly announced cuISS library.

Availability
Customers are currently evaluating Synopsys' agentic EDA and CAE capabilities with availability planned for the second half of 2026.

Follow Synopsys online for updates via our Newsroom, on LinkedIn, and on X.

Join Synopsys at the 2026 DAC Chips to Systems Conference
This week at DAC, Synopsys is showcasing AI-powered engineering solutions that enable customers to rapidly design from silicon to system with increased quality, efficiency, precision, and scale. Attendees can visit Synopsys' booth #631 for demonstrations of newly announced autonomous workflows. For a complete list of Synopsys sessions and activities at DAC 2026, visit the Synopsys DAC 2026 event page.

[1] Compared to traditional verification workflows not powered by AgentEngineer technology.

[2] AMS workflow leverages CCLS which delivers 3X gains in productivity.

[3] PrimeSim SPICE delivered approximately 18X faster overall wall-clock time by introducing NVIDIA GPUs compared to CPU-only workloads.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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Forward-Looking Statements
This press release contains forward-looking statements, which involve risks, uncertainties and other factors that could cause our actual results, time frames, or achievements to differ materially. Information on potential risks, uncertainties and other factors that could affect our results is included in filings we make with the SEC from time to time, including in the sections entitled "Risk Factors" in our latest Annual Report on Form 10-K and Quarterly Report on Form 10-Q.

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