Synopsys Enables AMD Instinct™ MI455X GPU Design with Comprehensive Multi-Die Solution

What's New: Synopsys joined the AMD Advancing AI 2026 event today to mark the launch of the AMD Instinct™ MI455X GPU, designed to power the next generation of AI infrastructure. For the new product series, AMD leveraged Synopsys' 3DIC Compiler, the industry's only exploration-to-signoff platform for multi-die/advanced package co-design and optimization. AMD accelerated their advanced package design with the platform's integrated multiphysics analysis and automated die-to-die and die-to-package routing.

The technologies used to develop advanced AI accelerators are also reshaping the infrastructure used to design them. Microsoft recently announced Azure HXv2, its next-generation technical and high-performance computing platform powered by 6th Gen AMD EPYC™ processors. Developed in collaboration with Synopsys and building on the companies' long-standing work optimizing Synopsys AI-powered EDA solutions on Azure, HXv2 is designed to help engineering teams scale performance-intensive semiconductor design workloads, accelerate throughput, and expand available capacity for demanding EDA workloads. Read the blog to learn more.

Why it Matters: As AI workloads drive unprecedented silicon complexity, developers need faster, more automated and integrated approaches to large-scale multi-die designs requiring high compute density, advanced packaging, and tightly coupled memory integration. For the AMD Instinct™ MI400 Series, Synopsys helped streamline development through unified co-design and optimization workflows that drove automation, accelerated system validation, and helped AMD deliver next-generation AI accelerator performance on an accelerated development schedule.

"AI infrastructure is entering a new era where continued advances in compute performance depend on innovation across silicon, packaging, memory, and system architecture," said Mark Papermaster, executive vice president and chief technology officer at AMD. "The new platform reflects that vision and the work required to bring increasingly sophisticated AI systems to market. Our close collaboration with Synopsys reflects a shared commitment to pushing the boundaries of AI compute and demonstrates what's possible when leading technology and engineering teams come together to enable next-generation platforms."

"In this era of unprecedented AI infrastructure buildout, engineering teams need solutions enabling extreme co-design to accelerate innovation cycles and deliver leading-edge performance with first-time right silicon," said Shankar Krishnamoorthy, chief product development officer at Synopsys. "From architecture through silicon bring-up, we are proud to have collaborated with AMD across emulation, verification, multi-die, multiphysics, and AI-powered solutions to deliver their bold MI455X design. It is a demonstration of how integrated, cross-domain development workflows and intelligent automation can transform ambitious architectures into production-ready AI platforms in record time."

A Closer Look:

- **Accelerating Development of a Next-Generation AI Platform:** Synopsys collaborated closely with AMD to help streamline design construction, implementation, and signoff for the AMD Instinct MI455X GPU. Using the Synopsys 3DIC Compiler platform, AMD leveraged a unified exploration-to-signoff flow that allowed fast heterogeneous integration, partitioning, prototyping, floorplanning, automated die-to-die and die-to-package routing, and integrated multiphysics analysis, while reducing reliance on manual workflows. AMD also leveraged Synopsys memory interface IP technologies to help address the demanding performance and data movement requirements of the MI455X platform.

- **Scaling Advanced Packaging with Confidence:** Integrated multiphysics analysis and quality of results-driven optimization helped AMD to overcome thermal, power, and electromagnetic challenges across the full system, supporting scalability, reliability, and design confidence.

- **Advancing Software Readiness and Reducing Integration Risk:** Synopsys ZeBu® emulation systems accelerated system validation and software readiness by enabling early validation of the GPU at the IP and sub-system level. For the SoC, ZeBu helped the software stack development and validation well before silicon availability. AMD utilizes advanced save-and-restore capabilities with ZeBu to improve emulator efficiency and supported rapid iterations during critical debug phases, allowing AMD to parallelize workflows and accelerate bring-up timelines. A lot of the performance validation workloads were also exercised on ZeBu's high fidelity and high-performance models to enable critical feedback into the design teams, when resolving bottlenecks discovered through complex and long software workloads. Collaboration between AMD and Synopsys' ZeBu teams for optimization of interfaces between ZeBu Software and AMD Vivado™ Design Suite fast tracked the delivery of complex high-capacity emulation models w up to 20 billion gates.

- **Accelerating Verification Closure and Improving Design Confidence:** AMD leveraged Synopsys VC Formal™, VCS® RTL simulation, and VC LP (low-power) verification solutions to accelerate bug detection, strengthen verification coverage, and validate critical functionality across both die-level and SoC-level environments. Combining formal verification and scalable simulation methodologies helped improve design quality and increase confidence in silicon readiness.

By creating a unified and automated design environment from concept to advanced packaging, AMD and Synopsys have established a proven foundation for large-scale multi-die designs and development.

Additional Resources:

- eBook: Multiphysics Fusion Technology for Multi-Die Designs Explained
- Brochure: Synopsys 3DIC Compiler Platform
- White Paper: Automated High-Speed Interface Routing in Multi-Die Designs

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