Synopsys Advances Power and Performance for AI and Multi-Die Designs on Latest Samsung Foundry Processes at SAFE Forum 2026

Highlights:

- New production-ready, AI-powered digital and analog flows are available for second-and third-generation 2nm processes accompanied by an expanded portfolio of certified interface IP, including for Samsung Foundry's automotive nodes.
- Unique Design Technology Co-Optimization (DTCO) initiatives for synthesis and layout, as well as signoff, are delivering meaningful power, performance, and area (PPA) enhancements.
- Customers are observing significant test efficiency improvements of up to 20% by leveraging AI-powered, silicon-based design and manufacturing test capabilities validated and deployed in collaboration with Samsung Foundry.

SUNNYVALE, Calif., May 28, 2026 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced at Samsung Advanced Foundry Ecosystem (SAFE) Forum 2026 its latest collaborations with Samsung Foundry on advanced nodes, including an expanded portfolio of production-ready, AI-powered EDA tools, certified interface IP, and silicon-based test capabilities, enabling customers to bring differentiated AI and multi-die designs to market faster and with measurably improved quality.

During his keynote at the event, Synopsys President and CEO Sassine Ghazi underscored the companies' long-standing collaboration to address compounding semiconductor engineering complexity, intense pressure for faster development cycles, and increasing costs. Ghazi emphasized that overcoming these challenges requires a fundamentally new approach where AI driven automation and multiphysics intelligence are fused across the entire design and manufacturing flow. Pointing to initiatives leveraging Synopsys AI-powered solutions and deep design and technology co optimization (DTCO), Ghazi said customers are bringing advanced silicon to market faster, while achieving meaningful gains in PPA and test efficiency, on Samsung Foundry's latest process nodes.

"Close alignment across design, test, and manufacturing are critical to the success of AI and multi-die designs on advanced nodes," said Hyung-Ock Kim, vice president and head of the Foundry Design Technology Team at Samsung Electronics. "Our continued close collaboration with Synopsys delivers silicon-based, customer-validated solutions that help our customers reduce design integration risk, improve silicon predictability, and move confidently from design to production for their most innovative solutions."

"As designs become more heterogeneous, customers need production-ready, silicon-proven solutions that address complexity and minimize risk from silicon to systems," said Ravi Subramanian, Chief Product Management Officer at Synopsys. "Our work with Samsung Foundry translates years of DTCO and silicon learning into enablement that helps our customers get their advanced designs to market quickly and with confidence."

The latest Synopsys and Samsung Foundry collaborations include:

- **New Synopsys Production-Ready Flows and Improved PPA on third-generation 2nm class process:** Synopsys AI-powered digital and analog flows are production-ready for third-generation 2nm class process, helping customers migrate to advanced Samsung Foundry nodes with speed and confidence. Through Synopsys and Samsung Foundry's continued DTCO initiatives, Synopsys Fusion Compiler™ on third-generation 2nm class process delivers measurable power and performance improvements validated with customers, compared to second-generation 2nm class process.
- **Silicon-Based Power and Performance Improvements During Signoff with Certified Multiphysics Capabilities:** New Synopsys PrimeShield™ Process Sensitivity Analysis and PVT Explorer support design-specific optimization and engineering change order (ECO) decisions during signoff, with demonstrated frequency improvement of up to 2.7% within 5% leakage current degradation respectively, informed by silicon feedback on 2nm class-based processes.[1] In addition, Synopsys Totem-SC is a newly certified electromigration (EM) and IR drop analysis solution on second-generation 2nm and 4nm class processes improving silicon design power integrity and reliability.
- **AI-Powered Test Improves Efficiency and Quality of Designs:** Synopsys and Samsung Foundry are applying silicon-proven methodologies to design for test (DFT) enablement and manufacturing test to reduce test cost and improve test quality for designs on advanced process nodes. For example, Synopsys TestMAX™ with AI-assisted automatic test pattern generation (ATPG) technologies (TSO.ai) validated and deployed in collaboration with Samsung Foundry teams, help reduce test patterns and test cycles up to 20% while preserving fault coverage on SoC and multi-die designs manufactured at Samsung Foundry. Additionally, physically aware tests and failure diagnosis at the die and multi-die level improve test quality and failure analysis turnaround time with results validated on silicon at Samsung Foundry.
- **Unified Exploration-to-Signoff Platform with Multiphysics Analysis Supporting Samsung's 3DIC Solution with Hybrid Copper Bonding Technology:** Synopsys and Samsung Foundry are enabling scalable 3D multi-die designs

through certified multiphysics signoff solutions delivered within Synopsys 3DIC Compiler, a unified exploration-to-signoff platform being validated on a Hybrid Copper Bonding (HCB) 3D test chip. The platform brings together planning, implementation, and multiphysics analysis to enable co-optimization across integrated compute, memory, and advanced packaging systems for Samsung's 3DIC solutions with HCB technology. By replacing manual, margin-based approaches with automated, AI-driven system optimization, the platform accelerates designer productivity while enhancing quality of results (QoR) for next-generation 3D AI designs.
- **Expanded IP Portfolio on Advanced and Automotive Nodes Decreases Design Integration Risk:** Synopsys offers the industry's broadest portfolio of IP across Samsung Foundry's advanced processes from 14nm, 8nm, and 5nm class processes to the latest titles for 4nm and second-generation 2nm supporting a wide range of applications for segments including high-performance computing, consumer electronics, mobile devices, and edge AI, as well as automotive applications at 5nm and 2nm class processes. Synopsys' broad portfolio of interface IP—including UCIe, PCIe 7.0, 112G/224G, MIPI, LPDDR6, DDR5 MRDIMM Gen2 and USB4, — and foundation IP—including embedded memories, logic libraries, GPIOs, as well as security IP and Silicon Lifecycle Management (SLM)— are optimized through the companies' long-standing collaboration to deliver trusted, low-risk solutions tailored to Samsung's processes to support faster time to market.

SAFE Forum 2026 showcases the continued, deep collaboration between Synopsys and Samsung Foundry, driven by companies' shared commitment to co-innovation and customer success at the most advanced nodes.

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Resources:

- **Overview:** Synopsys and Samsung Collaboration
- **Video:** Synopsys and Samsung: Delivering Technology Breakthroughs Together
- **Blog:** Accelerating Multi-Die Innovation with Samsung Foundry

[1] Compared to a previous version of Synopsys PrimeShield.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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