Synopsys Partners with TSMC to Power Next-Generation AI Systems with Silicon Proven IP and Certified EDA Flows

AI-powered digital, analog and verification flows and broad IP solutions deliver exceptional quality of results for TSMC advanced technologies

- Successful silicon bring-up of industry's first low-power M-PHY v6.0 IP on TSMC N2P, tape-out of 64G UCIe IP, and 224G IP speeds development of next-generation AI systems
- Ongoing collaboration on AI-powered digital, analog, and verification flows and power integrity platforms across TSMC advanced nodes to deliver optimized quality of results
- Collaboration on agentic run assistance in Synopsys Fusion Compiler improves PPA and design productivity on TSMC A14 using TSMC NanoFlex™ Pro architecture
- Synopsys 3DIC Compiler platform delivers productivity improvement for TSMC's CoWoS® technology at 5.5x reticle interposer sizes, enabling efficient 3D multi-die designs
- Multiphysics design enablement for COUPE supports next-generation co-packaged optics

SUNNYVALE, Calif., April 22, 2026 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) announced today major advances in silicon-proven IP, AI-powered EDA flows, and system-level enablement across TSMC's most advanced processes and packaging technology nodes, including the TSMC 3nm and 2nm families, as well as A16™ with Super Power Rail and A14.

By unifying intelligent digital, analog, and verification flows, advanced 3D multi-die design, and optical-to-electrical design capabilities, Synopsys helps engineers improve quality of multiphysics results and accelerate development cycles from silicon to systems for increasingly complex AI and high-performance computing designs.

"TSMC's most advanced process and packaging technologies are opening new frontiers for performance, bandwidth, and energy efficiency in AI and autonomous systems," said Michael Buehler-Garcia, Senior Vice President at Synopsys. "Through our deep collaboration, Synopsys is delivering AI-driven design flows, advanced multiphysics signoff, and a comprehensive portfolio of proven interface and foundation IP that help customers accelerate innovation and achieve outstanding quality of results."

"Our collaboration with Open Innovation Platform® (OIP) ecosystem partners like Synopsys continues to expand across TSMC's advanced nodes and 3DFabric® technologies to meet the rapidly growing demands of AI and high-performance computing," said Aveek Sarkar, Director of the Ecosystem and Alliance Management Division at TSMC. "By combining Synopsys' certified EDA solutions and IP portfolio with our latest process and packaging innovations, we are enabling customers to push the boundaries of performance, integration, and energy efficiency—driving leadership silicon for the next-generation of AI systems."

Advancing 3DFabric with Integrated Analysis and Signoff Flows forOptical, Electrical, and Thermal
To support the growing scale and complexity of multi-die designs,Synopsys and TSMC have enhanced enablement across TSMC's 3DFabric technologies, including TSMC-SoIC® and CoWoS® for 5.5x reticle interposer sizes. Synopsys' 3DIC Compiler, a unified exploration-to-signoff platform, enables designs usingTSMC's 3DFabric technologies with automation capabilities for productivity gains. Synopsys' 3DIC Compiler integrates withRedHawk-SC™, RedHawk-SC Electrothermal™, and Ansys HFSS™ software to deliver multiphysics analysis for thermal, power, and high-speed signal integrity.

Collaboration with Synopsys RedHawk-SC™ for digital power integrity,Synopsys Totem™ for analog power integrity, and HFSS-IC Pro for electromagnetic extraction expands from TSMC A16™ to A14. Synopsys Totem-SC™ provides analog power integrity signoff at ultrahigh-capacity for large N2-based designs and embedded memories, while Synopsys PathFinder-SC™ extends multi-die electrostatic discharge (ESD) signoff coverage to N2. Cloud-based multiprocessor and GPU acceleration further shortens turnaround time, enabling multiphysics design teams to iterate rapidly across complex, thermally constrained 3D assemblies.

Expanded multiphysics simulation and analysis capabilities strengthen coverage across photonic, electrical, and thermal domains. Enablement for COUPE spans Ansys Zemax OpticStudio® for optical path simulation, Ansys Lumerical™ for photonic device simulation, HFSS-IC Pro for electromagnetic extraction, and RedHawk-SC Electrothermal for thermal and electrical co-simulation. Together, these tools support the design of co-packaged optical solutions for high-bandwidth datacenter connectivity.

Accelerating Design Productivity and Time-to-Results
Synopsys is collaborating with TSMC on agentic run assistance in Synopsys Fusion Compiler™ on TSMC's A14 process using NanoFlex Pro architecture identifying timing improvement opportunities at different stages of the design flow for better quality of

results. In addition, enablement of AI-assisted physical verification in Synopsys IC Validator™ is on-going, aiming to accelerate the identification and resolution of DRC violations for faster tapeout quality results.

Extensive IP Portfolio on Advanced, Specialty, and Automotive TSMC Nodes
This year, Synopsys advanced its IP portfolio with significant innovations that strengthened its leadership in high-performance connectivity for AI, data center, edge, and automotive markets. Through a key photonics collaboration, the company introduced a 224G IP solution that enables co-packaged optical Ethernet and UALink to address the bandwidth demands of next-generation electro-optical systems. Synopsys also achieved multiple first-silicon milestones on TSMC's N5, N3P, and N2P processes— including PCIe 7.0, HBM4, 224G, DDR5 MRDIMM Gen2, LPDDR6/5X/5, UCIe 64G, and M-PHY v6.0 IP — establishing new levels in performance, power efficiency, and scalability.

Synopsys expanded its industry leading, silicon provenFoundation IP portfolio for TSMC's N3P and N2P processes, offering embedded memories, logic libraries, and IOs that enable low power data centers, AI accelerators, mobile networks, and advanced cloud computing platforms. With strong market traction, industry leading PPA, and a robust roadmap across compact "C" nodes from N6 to N3, Synopsys Foundation IP is ready to power the next wave of semiconductor innovation.

Additionally, Synopsys strengthened its automotive leadership with the launch of a complete UCIe IP ASILB solution on N5A, complementing its high reliability Interface and Foundation IP offerings on TSMC's N5A and N3A nodes for next-generation vehicle SoCs and reinforcing its momentum in the fast-growing automotive chiplet ecosystem.

Additional Resources

- Blog: Learn about Synopsys' silicon bring-up ofM-PHY v6.0 IP on TSMC's N2P process.
- Blog: Learn how Synopsys is deliveringLPDDR6 Read/Write Eyes at 10.67 Gb/s on TSMC's N2P process.
- Webinar: Gain executive-level insights from Synopsys, TSMC and others, into silicon and system engineering for AI hardware from experts at the forefront of these groundbreaking AI innovations
- Synopsys is also hosting several demonstrations at Booth #302 in TSMC 2026 Technology Symposium in North America. For more information, visit Synopsys TSMC Technology Symposium page.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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