

Synopsys Collaborates with TSMC to Drive the Next Wave of AI and Multi-Die Innovation

AI-Driven EDA and Broad IP Solutions Enable Differentiated Designs on TSMC Advanced Processes and SoIC Technologies

Key Highlights

- Certified digital and analog flows on the TSMC N2P and A16™ processes using TSMC NanoFlex™ architecture boost performance and speed analog design migration
- 3DIC Compiler platform and 3D-enabled IP enable multiple customer tape outs using advanced 3D stacking and CoWoS packaging technologies
- AI-optimized photonic flow for TSMC Compact Universal Photonic Engine (TSMC-COUPE™) technology enhances system design performance and addresses multi-wavelength and thermal requirements
- Industry's broadest IP portfolio, on TSMC N2/N2P, optimized for low power, speeds path to silicon success and reduces integration risk

SUNNYVALE, Calif., Sept. 24, 2025 /PRNewswire/ -- [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) announced today its ongoing close collaboration with TSMC to deliver multi-die solutions, encompassing advanced EDA and IP products, that support TSMC's leading-edge processes and packaging technologies, driving innovation in AI chip and multi-die design. The 3DIC Compiler exploration-to-signoff platform and IP, tuned for 3D packaging, along with the company's partnership with TSMC on design enablement has resulted in multiple customer tape-outs.

Building on Synopsys' continued collaboration with TSMC is the availability of certified digital and analog flows, along with the enabled Synopsys.ai™ on TSMC's N2P and A16™ processes using TSMC NanoFlex™ architecture. In addition, Synopsys provides robust automotive IP solutions for TSMC N5A and N3A processes and best-in-class Interface and Foundation IP solutions, delivering highest level of safety, security and reliability while enabling maximum performance with the lowest power for advanced chips.

"Our close collaboration with TSMC continues to empower engineering teams to achieve successful tape outs on the industry's most advanced packaging and process technologies," said Michael Buehler-Garcia, Senior Vice President at Synopsys. "With certified digital and analog EDA flows, 3DIC Compiler platform, and our comprehensive IP portfolio optimized for TSMC's advanced technologies, Synopsys is enabling mutual customers to deliver differentiated multi-die and AI designs with enhanced performance, lower power, and accelerated time to market."

"TSMC has been working closely with our long-standing Open Innovation Platform® (OIP) ecosystem partners like Synopsys to help customers achieve high quality-of-results and faster time-to-market for leading-edge SoC designs," said Aveek Sarkar, Director of the Ecosystem and Alliance Management Division at TSMC. "With the ever-growing need for energy efficient and high-performance AI chips, the OIP ecosystem collaboration is crucial for providing our mutual customers with certified EDA tools, flows and high-quality IP to meet or exceed their design targets."

Synopsys EDA Flows Deliver Enhanced Performance on TSMC Advanced Processes

Synopsys' analog and digital flows, along with the enabled Synopsys.ai, are certified on TSMC N2P and A16™ processes using TSMC NanoFlex™ architecture to help optimize performance, power, and to scale chip designs to advanced semiconductor technologies. Certified capabilities for designs on TSMC A16™ Super Power Rail (SPR) process improve power distribution and system performance, while maintaining thermal robustness of backside routing designs. Synopsys' pattern-based pin access methodology has been enhanced for TSMC A16™ node to deliver competitive area results. In addition, Synopsys is collaborating with TSMC on the design flow development for TSMC's A14 process and its first process design kit release scheduled for the later part of 2025.

[Synopsys IC Validator™](#) signoff physical verification solution is certified for TSMC A16™ process to support DRC and LVS checking. IC Validator's high-capacity elastic architecture seamlessly scales PERC rules to handle TSMC's N2P full-path electrostatic discharge (ESD) verification with improved turnaround time.

Advanced 3D Stacking and CoWoS Technologies Demonstrate Successful 3D Integration

Synopsys' 3DIC Compiler's unified exploration-to-signoff platform has been enabled to support the TSMC-SoIC® (SoIC-X) technology, including 3D stacked designs and silicon interposer and bridge with CoWoS® technologies, resulting in several customer tape outs. With 3DIC Compiler, customers can achieve higher productivity and faster turnaround times with the platform's automated UCle and HBM routing, TSV and bump planning, and multi-die signoff verification.

In addition, the ongoing collaboration between Synopsys and TSMC on silicon photonics has enabled an AI-optimized photonic IC flow for TSMC-COUPET[™] technology to deliver enhanced system performance and address multi-wavelength and thermal requirements in multi-die and AI designs.

Synopsys Industry-Leading IP Portfolio Paves the Way for Silicon Success

Synopsys is accelerating semiconductor innovation on next-generation TSMC's N2P/N2X processes with the industry's most comprehensive portfolio of best-in-class Foundation and Interface IP. The Synopsys IP portfolio enables the latest high-performance standards, including HBM4, 1.6T Ethernet, UCle, PCIe 7.0, and UALink, as well as a robust roadmap for automotive, IoT, and HPC applications. Synopsys provides a comprehensive suite of high-performance proven PHYs, embedded memories, high-density logic libraries, programmable IO, and NVM IP. With dedicated IP for N5A and N3A automotive nodes, along with advanced SRAM and Foundation IP for 5nm and 3nm SoCs, Synopsys empowers customers to meet the demanding requirements of next-generation designs across a broad range of markets.

Additional Resources

- Mutual customers of TSMC and Synopsys will be speaking about their experience with these new offerings to attendees of TSMC's OIP Forums. For information as to the topics and the joint presenters, please visit TSMC's OIP North America [web page](#).
- Learn about how Synopsys collaborates with TSMC to enable multiphysics and photonics design solutions [here](#).
- Synopsys is also hosting several demonstrations at Booth #204. For more information, visit [Synopsys TSMC OIP North America page](#).
- Additional information on IP for 3D Multi-Die Designs is available [here](#).

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP, simulation and analysis solutions, and design services. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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