Synopsys Accelerates AI and Multi-Die Design Innovation on Advanced Samsung Foundry Processes

Companies Strengthen Collaboration with Successful Tape Out of HBM Customer Design, Certified EDA Flows, and PPA-Optimized IP on Samsung's Advanced Technologies

Highlights

- Successful customer tape out of HBM3 design on SF2 process and I-CubeS technology leveraged Synopsys 3DIC Compiler to reduce turnaround time by 10X
- New Synopsys certified AI-driven digital and analog flows on SF2P accelerate development of high-performance designs
- AI-driven design technology co-optimization collaboration delivers superior PPA results on the SF2P process
- New Synopsys IP, including 224G, UCIe, MIPI and LPDDR6, on SF2P and SF4X speeds time-to-market for next-generation designs and offers a low-risk path to silicon-success

SUNNYVALE, Calif., June 16, 2025 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) announced today its ongoing close collaboration with Samsung Foundry to power the next generation of designs for advanced edge AI, HPC, and AI applications. The collaboration between the companies is helping mutual customers achieve successful tape-outs of their complex designs using Synopsys' 3DIC Compiler and Samsung's advanced packaging technologies with fast turnaround time. Mutual customers can improve power, performance and area (PPA) with certified EDA flows for SF2P process, and minimize IP integration risk with the high-quality portfolio of IP on Samsung's most advanced process technologies.

"The adoption of Edge AI applications is driving the need for advancements in semiconductor technologies to enable complex computational tasks, improve efficiency, and expand AI capabilities across various industries and applications," said John Koeter, senior vice president for the Synopsys IP Group. "Together with Samsung Foundry, we're enabling the most advanced AI processors across a broad spectrum of use cases from high-performance AI inference engines for data centers to ultra-efficient Edge AI devices like cameras and drones, all optimized for development on sub-2nm Samsung Foundry process technologies."

"Synopsys and Samsung have deepened their collaboration to optimize PPA for designs using Samsung's advanced technologies," said Hyung-Ock Kim, vice president and head of the Foundry Design Technology Team at Samsung Electronics "With Synopsys' AI-driven design flows certified for Samsung's SF2 and SF2P processes, customers can seamlessly integrate these solutions into their workflows. This collaboration also provides access to Synopsys' broad portfolio of IP optimized for Samsung's advanced nodes. Additionally, our joint efforts in delivering multi-die solutions, including 2.5D automated routing with Synopsys' 3DIC Compiler and Samsung's I-CubeS™ technology, are pushing the boundaries of innovation in this domain."

Successful Collaboration on Multi Die Design
Synopsys and Samsung are powering the most complex multi-die designs to enable mutual customers to rapidly deliver advanced technologies to the market. The companies' most recent collaboration includes a successful tape-out of a customer design using Synopsys' 3DIC Compiler, a unified exploration-to-signoff platform, and Samsung's I-CubeS 2.5D packaging technology, which allows several HBM stacked dies on a silicon interposer. In addition to substantially reducing HBM routing time to 4 hours, the Synopsys 3DIC Compiler improved worst-case eye opening by 6% for better performance and reliability. The ongoing projects leverage 3DIC Compiler's rapid 3D floorplanning with bump and Through-silicon via (TSV) planning and early thermal analysis, which is certified by Samsung for Samsung's X-Cube technology.

Collaboration on Design Technology Co-Optimization and EDA Flows
Synopsys and Samsung Foundry have had a decades-long collaboration using AI-driven design technology co-optimization (DTCO) to achieve superior PPA entitlement on SF2 and SF2P processes. Synopsys and Samsung also continue to collaborate on AI-driven flows using Synopsys ASO.ai™, resulting in a new schematic migration flow to efficiently migrate Samsung SF4 analog IPs to the SF2 process.

In addition, Synopsys' AI-driven digital and analog flows have achieved certification on Samsung Foundry's SF2P process with hypercells enablement for more efficient use of standard cell space, improving overall PPA, along with certified digital and analog flows for SF2/SF2P generation nodes. The flows, powered by the Synopsys.ai™ full-stack EDA suite, allow mutual customers to accelerate development of differentiated SoCs on Samsung's advanced process technologies.

Broad Portfolio of Synopsys IP for Samsung Foundry Speeds Time to Market
Synopsys and Samsung Foundry continue a strategic relationship to provide chipmakers with a comprehensive portfolio of high-quality IP optimized for performance, power, area, and latency across Samsung's advanced process nodes, from

14LPP/U, 8LPU, SF5A to the latest SF4X and SF2P/A. This collaboration supports a wide range of applications, including high-performance computing, consumer electronics, mobile devices, IoT, and automotive markets. Synopsys offers a broad portfolio of interface IP – such as and 224G, UCIe, PCIe 7.0, MIPI, LPDDR6X and USB4 – alongside foundation IP, including embedded memories, logic libraries, GPIOs, and PVT sensors, as well as security IP and Silicon Lifecycle Management (SLM) IP. By delivering trusted, low-risk solutions tailored to Samsung's processes, Synopsys enables mutual customers to accelerate time-to-market and gain a competitive edge for their advanced designs.

About Synopsys
Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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