Synopsys and Intel Foundry Propel Angstrom-Scale Chip Designs on Intel 18A and Intel 18A-P Technologies

Synopsys Production-Ready EDA Flows and Broadest IP Portfolio Deliver Leading PPAfor Intel Foundry's Advanced Processes and Packaging Technologies

Highlights

- Production-ready Synopsys digital and analog EDA flows for Intel 18A and Intel 18A-P technologies pave the way for broad adoption and accelerate development of high-performance designs; engaged in early design technology co-optimization for Intel 14A-E
- Optimized EDA reference flow with a unified exploration-to-signoff platform accelerates 2.5D/3D multi-die designs for Intel's EMIB-T advanced packaging technology
- Broadest portfolio of high-performance and low-power IP for Intel 18A and expanded Synopsys IP support for Intel 18A-P offers customers faster time-to-tapeout
- Announcing membership in Intel Foundry Accelerator Design Services Alliance and the new Intel Foundry Accelerator Chiplet Alliance to advance Intel Foundry adoption and innovation

SUNNYVALE, Calif., April 29, 2025 /PRNewswire/ -- At today's Intel Foundry Direct Connect 2025 event,Synopsys, Inc. (Nasdaq: SNPS) announced broad EDA and IP collaborations with Intel Foundry, including availability of its certified AI-driven digital and analog design flows for the Intel 18A process node and production-ready EDA flows for the Intel 18A-P process node with RibbonFET Gate-all-around transistor architecture and the industry's first commercial foundry implementation of PowerVia backside power delivery.

To drive multi-die design innovation forward, Synopsys and Intel Foundry are collaborating to enable Intel's new Embedded Multi-die Interconnect Bridge-T (EMIB-T) advanced packaging technology with an EDA reference flow powered by Synopsys 3DIC Compiler.

With its EDA flows, multi-die solution, and broad portfolio of Synopsys'foundation and interface IP on Intel 18A and Intel 18A-P, Synopsys is helping designers accelerate the development of highly optimized AI and HPC chip designs from silicon to systems.

In a keynote presentation at today's event,John Koeter, Senior Vice President, for the Synopsys IP Group, emphasized: "The successful collaboration between Synopsys and Intel Foundry is advancing the semiconductor industry with silicon to system design solutions to meet the evolving needs for AI and high-performance computing applications. Our production-ready EDA flows, IP, and multi-die solution, provides our mutual customers with comprehensive technologies to accelerate the development of chip designs that meet or exceed their requirements."

"Our continued collaboration with Synopsys enables engineering teams to accelerate 'systems of chips' innovation utilizing our unique systems foundry capabilities and optimized Synopsys EDA flows and IP on Intel 18A and Intel 18A-P process nodes to create differentiated designs with faster time-to-results," said Suk Lee, VP & GM of Ecosystem Technology Office, Intel Foundry. "Together, Intel Foundry and Synopsys are furthering design, manufacturing, and packaging co-optimization so our customers can meet the demands of the AI era."

Advancing Design Innovation with Comprehensive EDA and Multi-Die Solutions
Synopsys' digital and analog design flows are certified for Intel 18A process node and production-ready for Intel 18A-P enabling faster delivery of advanced-node SoCs with higher quality-of-results. Synopsys IP and EDA flows are also optimized for power and area on the Intel 18A and Intel 18A-P process nodes to take advantage of Intel's PowerVia backside power delivery network enabling thermal-aware implementation for PowerVia based designs. RibbonFET-driven synthesis and optimization enable designers to achieve differentiated power, performance, and area (PPA) on Intel 18A and Intel 18A-P process nodes. This is a result of an extensive design technology co-optimization (DTCO) effort between Intel Foundry and Synopsys engineering teams.

Synopsys and Intel Foundry are now engaging in early design technology co-optimization for Intel 14A-E to establish the readiness of Synopsys EDA flows for the next generation advanced node.

Synopsys and Intel have extended their collaboration to help mutual customers realize the PPA advantages of multi-die designs by enabling Intel's EMIB-T advanced packaging technology with Synopsys' 3DIC Compiler. EMIB-T combines the benefits of EMIB 2.5D and Foveros 3D packaging technologies for high interconnect densities at die sizes beyond the reticle limit. The EMIB-T reference flow is powered by Synopsys' unified exploration-to-signoff platform, allowing efficient EMIB-T

designs with early bump and TSV planning and optimization, and automated UCIe and HBM routing for high quality-of-results and fast 3D heterogeneous integration. Synopsys 3DIC Compiler allows feasibility and partitioning, prototyping and floorplanning, and multiphysics signoff in a single environment, allowing efficient design creation, implementation, optimization, and closure.

Synopsys Expands IP Portfolio for Advanced Angstrom-Level Designs
The introduction of angstrom-level processes will be crucial for next-generation AI and HPC chips, delivering optimized performance, power, area, and latency. To accelerate time-to-market for these designs, Synopsys is developing the industry's broadest IP portfolio for Interface, Foundation, and SLM (Silicon Lifecycle Management) IP on Intel 18A process node, including 224G Ethernet, PCIe 7.0, UCIe, USB4, embedded memories, logic libraries, IOs, and PVT sensors. Utilizing Intel's PowerVia backside power delivery technology, Synopsys IP will enhance power distribution and performance, enabling advanced and differentiated chip designs with Intel Foundry technologies.

Further Strengthening Intel Foundry Ecosystem to Accelerate Adoption and Innovation
Synopsys is further expanding its collaboration with Intel Foundry and the ecosystem by joining the Intel Foundry Accelerator Design Services Alliance and the new Intel Foundry Accelerator Chiplet Alliance. As a member of the latest Intel Foundry Alliance, Synopsys commits to offering its design services, in addition to optimized EDA tools and IP, to help customers accelerate their advanced chip designs. As a founding member of the new Intel Foundry Chiplet Alliance, Synopsys will further enable interoperability, manufacturability and design solutions supporting multi-die chips on Intel 18A.

Additional Resources
Synopsys is exhibiting and speaking at Intel Foundry Direct Connect today at the San Jose McEnery Convention Center, Booth #35. For more information, visit the Synopsys Intel Foundry Direct Connect event page.

About Synopsys
Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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