

Synopsys and TSMC Usher In Angstrom-Scale Designs with Certified EDA Flows on Advanced TSMC A16 and N2P Processes

AI-Driven Digital and Analog Flows, Multi-Die Innovations, and Broad IP Portfolio Deliver Unmatched Performance, Power and Area Advantages

Highlights

- Digital and analog design flows on TSMC A16™ and N2P deliver optimized performance and rapid analog design migration, enabled by Synopsys.ai
- Early collaboration on TSMC A14 process underway for Synopsys EDA flows development
- Collaboration on 3Dblox and TSMC's CoWoS® technologies for 5.5x reticle size packages, speeds integration of 3D stacked dies in next-generation AI chips
- Broad portfolio of Synopsys Foundation and Interface IP provides the lowest power on TSMC's N2/N2P processes
- Industry's most complete IP solutions for leading-edge standards, including HBM4, 1.6T Ethernet, UCle, PCIe 7.0, and UALink, enable high-bandwidth interfaces in data-intensive heterogeneous SoCs

SUNNYVALE, Calif., April 23, 2025 /PRNewswire/ -- [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) announced today its ongoing close collaboration with TSMC to deliver robust EDA and IP solutions for TSMC's most advanced processes and advanced packaging technologies to accelerate AI chip design and 3D multi-die design innovation.

Among the newest collaborations is availability of certified digital and analog flows on TSMC A16™ and N2P processes for design productivity and optimization, enabled by [Synopsys.ai™](#), and initial development of EDA flows on TSMC's A14 process. Synopsys and TSMC are also working on the tool certification for the newly announced TSMC N3C technology, building on the available N3P design solutions. To further accelerate semiconductor design for ultra-high-density 3D stacking, the Synopsys 3DIC Compiler, certified by TSMC, supports 3Dblox and enables TSMC's CoWoS® technology with 5.5x-reticle interposer sizes. In addition, Synopsys provides complete, silicon-proven IP solutions on TSMC's advanced processes, enabling designers to rapidly integrate the necessary functionality into their next-generation designs with the lowest power and maximum performance.

"Synopsys and TSMC are helping the semiconductor industry speed up the pace of innovation for Angstrom-scale designs by providing mission-critical EDA and IP solutions optimized for the most advanced process technologies," said Sanjay Bali, Senior Vice President of Strategy and Product Management at Synopsys. "Together, we are delivering future-ready solutions that empower engineers to push the boundaries of technology, achieve their design goals, and bring their products to market faster."

"Achieving high quality-of-results and faster time to market for advanced SoC designs are the cornerstone of the long-standing collaboration between TSMC and Synopsys," said Lipen Yuan, Senior Director of Advanced Technology Business Development at TSMC. "Collaborating closely with our Open Innovation Platform® (OIP) design ecosystem partners like Synopsys is vital to enable our mutual customers with certified flows and high-quality IP that are essential to meet or exceed their design targets on TSMC's advanced processes."

Jumpstart Designs on TSMC's Angstrom-Scale Processes

Synopsys' analog and digital flows are certified on TSMC A16™ and N2P processes to deliver optimized quality of results and accelerate analog design migration. Certified backside routing capabilities support customers to take advantage of the TSMC A16™ process, improving power distribution and design performance. Pattern-based pin access methodology has been enhanced for TSMC N2P and A16™ nodes to deliver competitive area results. To further optimize TSMC N2P designs, [Synopsys Fusion Compiler](#) is enhanced with a frequency optimization (Fmax) engine and intelligent legalization technology to boost performance.

In addition, the ongoing collaboration on Synopsys EDA flows for TSMC's A14 process demonstrates Synopsys' continued commitment to enable Synopsys EDA flows for robust, high-performance designs.

[Synopsys IC Validator™](#) signoff physical verification solution, including Design Rule Checks (DRC) and Layout Versus Schematic (LVS) checking, is certified for A16™ and N2P processes. In addition, IC Validator's high-capacity elastic architecture seamlessly scaled PERC rules to handle TSMC N2P electrostatic discharge (ESD) verification with improved turnaround time. Synopsys and TSMC also collaborated to certify IC Validator 3DIC solution for the 3Dblox standard.

Driving Successful Adoption of 3D Integration

Synopsys and TSMC are leading semiconductor innovation by enabling 3DIC Compiler to support TSMC's CoWoS® technology for unprecedented 5.5x reticle interposer sizes, which has been proven in customer designs. The collaboration helps mutual customers meet demanding compute performance requirements for next-generation HPC and AI chips using wafer-on-wafer and chip-on-wafer advanced packaging. For a seamless migration to 2.5D and 3D multi-die designs, Synopsys' 3DIC Compiler supports 3Dblox and provides a single environment for analysis-driven feasibility exploration, prototyping, and floorplanning. The platform offers high throughput routing automation to enable ultra-high-density interconnects and increased productivity. 3DIC Compiler integrates multi-physics analysis and signoff solutions combined with Ansys simulation technologies for power, thermal, and signal integrity analysis.

Reduce Risk with Industry's Broadest Interface and Foundation IP Portfolio

Adopted by multiple customers, Synopsys offers best-in-class Interface and Foundation IP solutions for TSMC's N2/N2P processes, enabling maximum performance with the lowest power for advanced HPC, edge, and automotive chips. With successful deployment of Synopsys IP in thousands of designs, Synopsys and TSMC continue to enable mutual customers to reduce integration risk while meeting stringent power, performance, and area targets. Synopsys' complete, silicon-proven IP solutions for leading standards such as 1.6T Ethernet, PCIe 7.0, UCle, HBM4, USB4, DDR5, LPDDR6/5X/5, and MIPI, along with embedded memories, logic libraries and IOs, provide a low-risk path for first pass silicon success.

Additionally, Synopsys has expanded its IP solutions portfolio to include standards-based UALink and Ultra Ethernet IP, which is built on industry-leading PCIe and Ethernet IP. Synopsys' silicon-proven 224G PHY IP, a backbone of high-performance computing (HPC) systems, has demonstrated wide ecosystem interoperability including optical and copper connections, enabling an early start on advanced HPC and AI chips for upcoming standards.

Additional Resources

Synopsys is hosting several demonstrations at the TSMC Tech Symposium Forum today in Santa Clara at Booth #408. For more information, visit the [Synopsys TSMC Tech Symposium event page](#).

About Synopsys

Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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