Synopsys Announces Industry's First Ultra Ethernet and UALink IP Solutions to Connect Massive AI Accelerator Clusters

Best-in-Class Silicon IP Addresses Industry Need for Open Standard Solutions to Scale AI Accelerator Infrastructure

Highlights

- Synopsys Ultra Ethernet IP solution will enable up to 1.6 Tbps of bandwidth to connect up to one million endpoints
- Synopsys UALink IP solution will offer up to 200 Gbps throughput per lane, linking up to 1,024 accelerators
- New Ultra Ethernet and UALink IP is built on Synopsys' industry-leading Ethernet and PCIe IP, which together have enabled more than 5,000 successful customer tapeouts
- Industry leaders, including AMD, Astera Labs, Juniper Networks, Tenstorrent, and XConn are collaborating with Synopsys to scale the HPC and AI accelerator ecosystem

SUNNYVALE, Calif., Dec. 11, 2024 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced the industry's first Ultra Ethernet IP and UALink IP solutions, including controllers, PHYs, and verification IP, to meet the demand for standards-based, high-bandwidth, and low-latency HPC and AI accelerator interconnects. As hyperscale data center infrastructures evolve to support the processing of trillions of parameters in large language models, they must scale to hundreds of thousands of accelerators with highly efficient and fast connections. Synopsys Ultra Ethernet and UALink IP will provide a holistic, low-risk solution for high-speed and low-latency communication to scale-up and scale-out AI architectures.

"For more than 25 years, Synopsys has been at the forefront of providing best-in-class IP solutions that enable designers to accelerate the integration of standards-based functionality," said Neeraj Paliwal, senior vice president of IP product management at Synopsys. "With the industry's first Ultra Ethernet and UALink IP, companies can get a head start on developing a new generation of high-performance chips and systems with broad interoperability to scale future AI and HPC infrastructure."

Synopsys Ultra Ethernet IP Solution Supports Scaling Out to One Million Endpoints
Advanced capabilities of the new Synopsys Ultra Ethernet IP solution include:

- **IP solution to scale out backend networks:** Consisting of PHY, MAC and PCS controller, and verification IP, the Synopsys Ultra Ethernet IP solution offers a low-risk path for designers developing systems that can support up to one million endpoints in a single network.
- **Best-in-class 224G Ethernet PHY IP**: The silicon-proven Synopsys 224G Ethernet PHY IP, which supports the Ultra Ethernet protocol, has demonstrated broad interoperability as shown at multiple tradeshows including ECOC, OFC, and DesignCon.
- **Patented error correction implementation:** The Synopsys Ultra Ethernet MAC and PCS controller IP provides up to 1.6 Tbps of bandwidth with ultra-low latency, enabling the real-time processing needed for AI workloads.
- **Seamless integration:** The MAC and PCS IP support an interface to the higher layers of the Ultra Ethernet stack providing a full silicon implementation for switches, AI accelerators and smart NICs.
- **Accelerated verification and validation**: The Synopsys Ultra Ethernet verification IP helps ensure protocol adherence to rapidly evolving standards, enabling faster and more efficient validation of AI and HPC systems.

"Juniper has already introduced the industry's first 800GbE capability with its PTX10002-36QDD Packet Transport Router, which utilizes our proprietary Express 5 ASIC with Synopsys Ethernet IP," said Debashis Basu, senior vice president of Juniper Engineering. "We will continue to partner with Synopsys and leverage the latest technologies from the Ultra Ethernet Consortium (UEC) to transition into the 1.6TbE era. This indicates our ongoing innovation in high-speed networking to achieve our goal to significantly improve scale, reliability, and performance in data center networks. This is particularly important as AI workloads continue to grow exponentially, making such networks much more efficient and cost-effective."

Synopsys UALink IP Solution Enables Massive Increases in AI Compute Capacity
Advanced capabilities of the new Synopsys UALink IP solution include:

- **IP solution to scale up computing fabrics:** Consisting of PHY, controller, and verification IP, the Synopsys UALink IP solution speeds time-to-market for designers developing systems that can support up to 1,024 AI accelerators.
- **Efficient, high-speed data transfers:** Engineered for data-intensive AI workloads, the low-power and high-bandwidth Synopsys UALink PHY IP provides 200 Gbps per lane.
- **Latency-optimized with memory sharing capabilities**: Synopsys UALink Controller IP helps mitigate critical bottlenecks of AI hardware infrastructure via shared memory access from accelerator to accelerator.
- **Built-in protocol checks:** The Synopsys UALink Verification IP, combined with Synopsys hardware-assisted verification

solutions, provides quick and reliable verification for AI hardware.

"Synopsys has decades of expertise in contributing to the industry's essential interconnect standards and in delivering widely adopted high-speed interface IP," said Kurtis Bowman, chairperson of the board at UALink Consortium. "We appreciate Synopsys' commitment to enabling UALink IP to create a scalable, high-performance data center ecosystem for designers to meet the growing demands of AI models."

Additional Industry Leaders Collaborate with Synopsys to Enable AI Accelerator Interconnects at Scale
"Advancing AI technology requires industry-wide efforts to create high-performance solutions essential for the future of data centers," said Robert Hormuth, corporate vice president, architecture and strategy, data center solutions group at AMD. "The introduction of Synopsys' Ultra Ethernet and UALink IP, alongside AMD high-performance processors, highlights the commitment to create an open, robust, and scalable ecosystem for large-scale AI and high-performance computing."

"The progress of AI technology relies on industry collaboration to deliver scalable and power-efficient high-performance accelerator fabrics," said Chris Petersen, fellow, technology and ecosystems at Astera Labs. "New interconnect technologies such as UALink will help support the rapid growth and complexity of AI and HPC workloads. We congratulate Synopsys on the delivery of its new IP solutions to enable this critical connectivity ecosystem."

"Participating in defining and developing an open standards-based AI systems communications is an important part of Tenstorrent's charter. The low latencies and high bandwidths of the upcoming UEC and UALink standards will enable ultra-efficient interfaces supporting AI compute with multi-trillion parameter models," said David Bennett, chief customer officer at Tenstorrent. "Tenstorrent's RISC-V chips and Synopsys' new UALink and Ultra Ethernet IP will enable the largest AI accelerator clusters."

"To keep pace with the exponential growth in AI model parameters and compute requirements, hyperscalers need to address immense connectivity challenges," said Gerry Fan, CEO at XConn. "With XConn's UALink switches and Synopsys' new UALink IP, system architects can deploy high-performance, standards-compliant systems for future AI computing and networking architectures."

Availability & Additional Resources
The Synopsys Ultra Ethernet IP solution, including MAC and PCS, PHY, and verification IP, is scheduled to be available in the first half of 2025. The Synopsys UALink IP solution, including controller, PHY, and verification IP, is scheduled to be available in the second half of 2025.

- Learn more about Synopsys Ultra Ethernet IP
- Learn more about Synopsys UALink IP
- Blog: Enabling Massive AI Clusters with the Industry's First Ultra Ethernet and UALink IP Solutions
- Video: Scaling AI Networks with Synopsys Ultra Ethernet and UALink IP

About Synopsys
Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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