

Synopsys and TSMC Pave the Path for Trillion-Transistor AI and Multi-Die Chip Design

Optimized EDA and IP Solutions Deliver Enhanced Compute Performance, Power and Engineering Productivity for TSMC N2 and A16 Processes

Highlights

- Production-ready AI-driven EDA flows, powered by Synopsys.ai, on N2 deliver exceptional quality of results and accelerate design node migration for industry leaders
- Developing new backside power delivery capabilities on TSMC's A16 to enable efficient power distribution and system performance
- Joint TSMC, Synopsys and Ansys multi-physics flow supporting CoWoS interposer packaging addresses thermal and power integrity challenges
- Synopsys 3DSO.ai delivers AI-driven system analysis for maximum quality of results with support for TSMC's 3DFabric
- New development of 40G UCIe, HBM4 and 3DIO IP on advanced TSMC nodes optimizes latency, power, performance and area

SUNNYVALE, Calif., Sept. 25, 2024 /PRNewswire/ -- [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) today announced its continued, close collaboration with TSMC to deliver advanced EDA and IP solutions on TSMC's most advanced process and 3DFabric technologies to accelerate innovation for AI and multi-die designs. The relentless computational demands in AI applications require semiconductor technologies to keep pace. From an industry leading AI-driven EDA suite, powered by [Synopsys.ai™](#) for enhanced productivity and silicon results to complete solutions that facilitate the migration to 2.5/3D multi-die architectures, Synopsys and TSMC have worked closely for decades to pave the path for the future of billion to trillion-transistor AI chip designs.

"TSMC is excited to collaborate with Synopsys to develop pioneering EDA and IP solutions tailored for the rigorous compute demands of AI designs on TSMC advanced process and 3DFabric technologies," said Dan Kochpatcharin, head of the Ecosystem and Alliance Management Division at TSMC. "The results of our latest collaboration across Synopsys' AI-driven EDA suite and silicon-proven IP have helped our mutual customers significantly enhance their productivity and deliver remarkable performance, power, and area results for advanced AI chip designs.

"For decades, Synopsys has closely collaborated with TSMC, providing mission-critical EDA and IP solutions spanning all generations of TSMC's most advanced nodes," said Sanjay Bali, senior vice president of EDA product management at Synopsys. "This partnership has been instrumental in helping our mutual customers accelerate their innovation in the AI era and advance the future of semiconductor designs. Together, we are pushing the boundaries of what's possible, enabling groundbreaking advancements in performance, power efficiency, and engineering productivity."

Synopsys AI-Driven EDA Design Flows Boost PPA and Engineering Productivity

Industry leaders have embraced Synopsys AI-driven EDA flows, powered by Synopsys.ai for their advanced chip designs on N2.

"Synopsys' certified Custom Compiler and PrimeSim solutions provide the performance and productivity gains that enable our designers to meet the silicon demands of high-performance analog design on the TSMC N2 process," said Ching San Wu, Corporate VP at MediaTek. "Expanding our collaboration with Synopsys makes it possible for us to leverage the full potential of their AI-driven flow to accelerate our design migration and optimization efforts, improving the process required for delivering our industry-leading SoCs to multiple verticals."

In addition, Synopsys is collaborating with TSMC on the new backside routing capabilities supporting TSMC's A16 process in the Synopsys digital design flow to address power distribution and signal routing for design performance efficiency and density optimization. Interoperable process design kits (iPDKs) and [Synopsys IC Validator™](#) physical verification runsets are available for design teams to handle the increasing complexity of physical verification rules and efficiently transition designs to TSMC N2 technology.

To further accelerate chip design, Synopsys and TSMC have enabled Synopsys EDA tools on the cloud through TSMC's Cloud Certification, providing mutual customers with cloud-ready EDA tools that deliver accurate quality of results and seamlessly integrate with TSMC's advanced process technology. Synopsys' cloud-certified tools include synthesis, place and route, static timing and power analysis, transistor-level static timing analysis, custom implementation, circuit simulation, EMIR analysis and design rule checking.

Advancing Multi-Die Innovation with Comprehensive EDA Solutions

Synopsys, Ansys and TSMC have collaborated to address the complex multi-physics challenge for multi-die designs with a comprehensive system analysis flow by leveraging their prime solutions. The most recent flow based on [Synopsys 3DIC Compiler](#) unified exploration-to-signoff platform, which integrates 3DSO.ai, combined with Ansys RedHawk-SC™ power integrity signoff platform for digital and 3D integrated circuits, enhances the thermal and IR-aware timing analysis. Synopsys 3DIC Compiler is a TSMC-certified platform supporting 3Dblox, TSMC's 3DFabric, which includes TSMC-SolC® (System on Integrated Chips) and CoWoS packaging technologies.

"Our collaboration with Synopsys and TSMC exemplifies our collective commitment to driving innovation and enabling the future of AI and multi-die chip design," said John Lee, vice president and general manager, semiconductor, electronics and optics business at Ansys. "Together, we are tackling the multi-physics challenges inherent in multi-die architectures, helping our mutual customers achieve golden signoff accuracy for chip, package, and system-level effects within the Synopsys design environment on the latest TSMC technologies."

Reduce Risk with Silicon-Proven IP

Synopsys' comprehensive multi-die test solutions, available with the Synopsys UCle and HBM3 IP, ensure multi-die package health during manufacturing test and in-field. In collaboration with TSMC, Synopsys has taped out a test chip utilizing TSMC's CoWoS interposer technology with full support for test, monitor, debug, and repair capabilities. The diagnosis, traceability, and mission mode signal integrity monitoring allow in-design, in-ramp, in-production, and in-field optimization for purposes such as predictive maintenance. The Monitoring, Test, and Repair (MTR) IP for UCle PHY provides testability at the die, die-to-die interface and multi-die package levels.

Synopsys has achieved multiple silicon successes for UCle and HBM3 IP solutions across N3E and N5 process technologies, accelerating IP integration and minimizing risk. Latest developments of the Synopsys UCle IP, operating up to 40G, allows maximum bandwidth and energy efficiency without the need for additional area while the HBM4 and 3DIO IP solutions accelerate heterogeneous integration of 3D stacked-dies on TSMC's advanced processes.

Additional Resources

- LinkedIn article: [Synopsys-TSMC Successful Tapeout of a Test Chip Featuring a Multi-Die Design Using TSMC's CoWoS Technology](#)
- Synopsys is hosting several demonstrations at the TSMC OIP Ecosystem Forum today in Santa Clara at [Booth #204](#)

About Synopsys

Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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