

Synopsys Powers World's Fastest UCIe-Based Multi-Die Designs with New IP Operating at 40 Gbps

Complete Synopsys 40G UCIe IP Solution Delivers Maximum Bandwidth for Die-to-Die Connectivity in High-Performance AI Data Center Chips

Highlights

- Industry's first complete 40G UCIe IP solution, including controller, PHY, and verification IP, enables fast connectivity between heterogeneous and homogeneous dies
- Synopsys 40G UCIe PHY IP offers 25% higher bandwidth than the UCIe specification without impact on energy efficiency and silicon footprint
- Integrated signal integrity monitors and testability features improve multi-die package reliability and enable in-field monitoring throughout the silicon lifecycle
- Synopsys 40G UCIe IP is built on a silicon-proven architecture with interoperability success in multiple advanced foundry processes

SUNNYVALE, Calif., September 9, 2024 – [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) today announced the industry's first complete [UCIe IP solution operating at up to 40 Gbps](#) per pin to address the increased compute performance requirements of the world's fastest AI data centers. The UCIe interconnect, the de facto standard for die-to-die connectivity, is critical for high-bandwidth, low-latency die-to-die connectivity in multi-die packages, enabling more data to travel efficiently across heterogeneous and homogeneous dies, or chiplets, in today's AI data center systems. Synopsys' 40G UCIe IP supports both organic substrate and high-density, advanced packaging technologies to give designers the flexibility to explore the packaging options that best fit their needs. The complete Synopsys 40G UCIe IP solution, including PHY, controller, and verification IP, is a key component of Synopsys' comprehensive and scalable multi-die solution for fast heterogeneous integration from early architecture exploration to manufacturing.

"Heterogeneous integration with high-bandwidth die-to-die connectivity gives us the opportunity to deliver new memory chiplets with the efficiency needed for data-intensive AI applications," said Jongwoo Lee, vice president of the System LSI IP Development Team at Samsung Electronics. "Leveraging Synopsys' new 40G UCIe IP, we can extend our collaboration to develop industry-leading chiplet solutions for tomorrow's high-performance data centers."

"Launching the industry's first complete 40G UCIe IP solution underscores Synopsys' continued investment in advancing semiconductor innovation," said Michael Posner, vice president of IP product management at Synopsys. "Our active contribution to the UCIe consortium has enabled us to deliver a robust UCIe solution that helps our customers successfully develop and optimize their multi-die designs for high-performance AI computing systems."

Advanced capabilities of the new Synopsys 40G UCIe IP solution include:

- **Simplified Solution Eases IP Integration:** Single reference clock feature simplifies the clocking architecture and optimizes power. For ease of use and integration, the IP speeds-up die-to-die link initialization without the need to load the firmware.
- **Silicon Health Monitoring Enhances Multi-Die Package Reliability:** To ensure reliability at the die, die-to-die, and multi-die package levels, Synopsys 40G UCIe IP offers test and silicon lifecycle management (SLM) features. The monitoring, test, and repair IP and integrated signal integrity monitors enable diagnosis and analysis of the multi-die package from in-design to in-field.
- **Successful Ecosystem Interoperability:** For on-chip interconnect needs of the latest CPUs and GPUs, Synopsys 40G UCIe IP supports the most popular [on-chip interconnect fabrics including AXI, CHI chip-to-chip, streaming, PCI Express, and CXL](#). For successful interoperability, the IP is compliant with the UCIe 1.1 and 2.0 standards, which Synopsys helps to develop and promote as an active member of the UCIe Consortium.
- **Pre-Verified Design Reference Flow:** The combination of Synopsys UCIe IP and Synopsys 3DIC Compiler, a unified exploration-to-signoff platform, is used in Synopsys' pre-verified design reference flow that includes all the required design collateral such as automated routing flow, interposer studies, and signal integrity analysis.
- **Broad IP Solutions for Multi-Die Designs:** In addition to UCIe IP and high-speed SerDes, Synopsys offers HBM3 and 3DIO IP to enable high-capacity memory and 3D packaging.

Availability & Additional Resources

The Synopsys 40G UCle IP will be available in late 2024 for multiple foundries and processes.

- [Web: Synopsys UCle IP Solution](#)
- [Blog: Synopsys Introduces Industry's First 40G UCle IP Solution to Power High-Performance Multi-Die Designs](#)
- [Blog: UCle 2.0 - Setting the Tone for Chiplet Interoperability](#)

About Synopsys

Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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