

Synopsys Achieves Certification of its AI-driven Digital and Analog Flows and IP on Samsung Advanced SF2 GAA Process

Production-Ready Design Flows, Multi-Die Solution, and Synopsys IP Deliver a Proven Path to Unparalleled Power and Performance for AI and HPC Designs

Highlights

- Test chip tapeouts validate product readiness of certified digital and analog design flows for Samsung Foundry SF2/SF2Z process
- Collaboration on design techniques for SF2, including backside power and nanosheet optimization delivers more efficient power distribution
- Synopsys IP, now available and silicon proven on Samsung SF2, reduces integration risk and accelerates silicon success
- Qualified multi-die design reference flow and UCle IP for SF2 process accelerates 2.5D/3D heterogeneous integration
- Expanded collaboration on Synopsys.ai includes Synopsys ASO.ai for accelerated analog design migration with new analog design migration reference flow for Samsung's GAA processes

SUNNYVALE, Calif., June 12, 2024 /PRNewswire/ -- [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) today announced that its AI-driven digital design and analog design flows have achieved certification on Samsung Foundry's SF2 process with multiple test chip tapeouts. The reference flows, powered by the [Synopsys.ai™ full-stack EDA suite](#), enhance PPA, boost productivity, and accelerate analog design migration for Samsung Foundry's latest Gate-All-Around (GAA) process technologies. The Samsung SF2 process was optimized using Synopsys' AI-driven design technology co-optimization (DTCO) solution which delivered significantly superior performance, power, and area (PPA) for the process compared to optimization without the use of AI. Building on this success, the same co-optimization techniques will be applied for Samsung's advanced SF1.4 process.

"The demand for custom SoCs in the era of pervasive intelligence requires extensive ecosystem collaboration to help customers accelerate their innovation and silicon success on Samsung's SF2 and next-generation SF1.4 processes," said Sanjay Bali, vice president of product management and strategy for the EDA Group at Synopsys. "Achieving certification and multiple successful tapeouts of our digital and analog flows, powered by Synopsys.ai, on the SF2 process, combined with proven Synopsys IP provides designers with a trusted path to meeting their aggressive design goals for a faster time to market."

"Synopsys and Samsung have worked closely for decades to help our mutual customers achieve their most complex design requirements," said Sangyun Kim, Vice President and head of Foundry Design Technology Team at Samsung Electronics. "This latest collaboration milestone with Synopsys on AI-driven EDA flows and broad IP portfolio development is a testament to our ongoing efforts to address the industry's growing demand for high performance computing with significant PPA gains. Working together we validated our PPA results using Synopsys' certified digital flow, achieving 12% higher performance, 25% reduction in power, and 5% area reduction compared to the base design."

Collaboration on AI-driven EDA Flows

Synopsys and Samsung are closely collaborating on AI-driven flows, including [Synopsys DSO.ai™](#) for design productivity and PPA optimization, and [Synopsys ASO.ai™](#) for faster analog design migration. This collaboration has resulted in a new analog design migration reference flow using Synopsys ASO.ai for Samsung's FinFET to GAA processes, enabling designers to efficiently migrate Samsung 8nm analog IPs to SF2 process, adding to Synopsys' established flows on Samsung's 14nm to 8nm/SF5 processes.

New Design Techniques and Methodology for Advanced GAA Processes

Synopsys' continued innovation helps mutual customers benefit from new design techniques including backside routing, local layout effect-aware methodology, and nanosheet cell design, to help customers meet their design goals for power, performance, and area on Samsung SF2 process family. In addition, integrating backside routing and the super-cell approach using Synopsys' digital implementation and signoff tools enables designers to increase transistor performance efficiency and density, optimize power consumption, and reduce area by up to 20% for Samsung's SF2Z process technology compared to chips without backside routing capabilities.

Accelerate SoC and Multi-Die Designs

Synopsys IP for Samsung standard and automotive processes from SF2 to SF14LPU delivers a competitive edge for chipmakers looking to reduce integration risk and accelerate time to silicon success for automotive, mobile, high-performance computing (HPC) and multi-die designs. The industry's broadest portfolio of standards-compliant, silicon-proven interface IP for advanced Samsung processes, including PCIe 6.0/5.0/4.0, DDR5, LPDDR5X/5/4X, MIPI M-PHY G5, eUSB2, USB 3.2/3.1, and DisplayPort enables wide interoperability for commonly used protocols. To accelerate integration of chiplets in multi-die

packages, Synopsys UCle IP has taped out in SF2 and SF4x, and achieved silicon success in SF5A process technologies, to deliver robust die-to-die connectivity with low power and low latency. Synopsys Foundation IP, including embedded memories, logic libraries and GPIOs, is also proven in silicon to deliver leading power, performance, and area in a range of Samsung process technologies.

Mutual customers can accelerate the development of multi-die designs using [Synopsys 3DIC Compiler](#), a unified exploration-to-signoff platform for 2.5D and 3D heterogeneous integration and advanced packaging. Qualified for Samsung Foundry's SF2 process, Synopsys 3DIC Compiler supports Samsung's advanced silicon processes, packaging technologies, and 3DCODE standard. Synopsys is an active member of the Samsung Foundries' MDI Alliance, helping mutual customers achieve a successful transition to 2.5D and 3D advanced packaging designs.

About Synopsys

Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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