Synopsys Announces New AI-Driven EDA, IP and Systems Design Solutions At SNUG Silicon Valley

CEO Sassine Ghazi Discusses Unprecedented Opportunity in Era of Pervasive Intelligence

News Highlights:

- Announces Synopsys.ai customer momentum with applications including DSO.ai and VSO.ai delivering significant improvements in PPA, turn-around time, and more;
- Drives multi-die design innovation with Platform Architect - Multi-Die and new Synopsys.ai capability, 3DSO.ai, for AI-driven 3D design space optimization using native thermal analysis;
- Unveils new state-of-the-art hardware-assisted verification systems for faster, higher capacity emulation and prototyping;
- Announces new Synopsys Cloud Hybrid Solution, enabling seamless "burst to cloud" EDA capability;
- Further expands Synopsys' broad semiconductor IP portfolio with acquisition of Intrinsic ID

SUNNYVALE, Calif., March 20, 2024 /PRNewswire/ -- Today Synopsys, Inc. (Nasdaq: SNPS) kicked off its annual flagship Synopsys User Group (SNUG) conference in Silicon Valley at the Santa Clara Convention Center with a keynote presentation by Synopsys president and CEO Sassine Ghazi. Ghazi discussed the unprecedented innovation opportunities and challenges that technology R&D teams face in this era of pervasive intelligence. He also announced new EDA and IP solutions aimed at maximizing the capabilities of the global technology engineering teams, from silicon to systems, that Synopsys serves.

"The rapid advancement of AI, silicon proliferation, and software-defined systems are driving the era of pervasive intelligence, where technology is seamlessly integrated into our lives, bringing with it unprecedented opportunity and greater compute, energy, and design challenges for the technology industry," said Ghazi. "Synopsys is committed to collaborating with the ecosystem to address these challenges, while delivering the trusted silicon to systems design solutions our customers need to expand R&D capacity, maximize productivity, and power their innovations for this new era."

Jensen Huang, founder and CEO of NVIDIA, joined Ghazi on stage and discussed the companies' shared history of innovation, impact of AI on the semiconductor industry, and newly announced technology collaborations. Today's events also featured video commentary from additional customers and partners including AMD, Ampere, Arm, Astera Labs, Intel Foundry Services, Microsoft, Tesla, TSMC, and Samsung who each explained the important role Synopsys plays in their success.

Below is a summary of Synopsys technology news and announcements made during today's keynote presentation. More information is available in the SNUG Newsroom.

Synopsys.ai Gains Momentum: Synopsys DSO.ai and VSO.ai Delivering Stunning Customer Results

Today's keynote showcased the strong momentum for Synopsys.ai, the company's AI-driven full-stack EDA suite. Ghazi said Synopsys.ai usage is expanding rapidly, led by DSO.ai, Synopsys' industry-first AI application for optimizing layout implementation workflows, and VSO.ai, the industry-first, AI-driven verification solution.

Ghazi said Synopsys.ai has achieved hundreds of tape-outs to date and is delivering stunning customer results including a more than 10% boost in performance, power, area (PPA), up to 10X faster turn-around time and double-digit improvements in verification coverage, 4X faster test with the same coverage, and 4x faster analog circuit optimization when compared to optimization without the use of AI.

Synopsys has pioneered AI capabilities across the Synopsys.ai suite, adding verification, test, and analog capabilities, all commercially available and ramping. The company's AI innovation is continuing with the development of Generative AI capabilities across the stack, starting with Synopsys.ai Copilot, and today's announcement of a new Synopsys.ai capability for 3D design space optimization.

Accelerating Multi-die Innovation with New 3DSO.ai for 3D Design Space Optimization, Architectural Exploration, and Silicon-Proven UCIe IP

Furthering its efforts to drive the mainstream adoption of multi-die designs, Synopsys is introducing 3DSO.ai, a new AI-driven capability delivering unparalleled productivity gains while maximizing system performance and quality of results. Built natively into Synopsys 3DIC Compiler, a unified exploration-to-signoff platform, and powered by fast integrated analysis engines, 3DSO.ai offers optimization for signal integrity, thermal integrity, and power-network design. Synopsys 3DSO.ai is now available to early adopters.

Ghazi also highlighted Synopsys' industry-first solution for early architecture exploration of multi-die systems, Synopsys

Platform Architect - Multi-Die. Platform Architect accelerates design timelines, delivering a dramatic 6-12 month "shift left" from RTL for the analysis of performance and power, while accounting for the interdependencies between multiple dies. It allows systems architects to automate modeling, simulation, and analysis for early partitioning decisions, and helps customers avoid costly, late-stage changes and respins.

Additionally, he emphasized the importance of multi-die solutions, spotlighting Intel's Pike Creek, the world's first silicon-proven UCIe-connected and a result of collaboration between Intel, TSMC and Synopsys. The chip, a collaboration between Intel, TSMC and Synopsys, includes an Intel UCIe IP die built on its Intel 3 process node and a Synopsys UCIe IP die built on the TSMC N3E process. Ghazi commented, "This is the future of the semiconductor industry: multiple fabs, multiple sets of industry standard UCIe IP, and modern EDA packaging solutions."

Advancing State-of-the-Art Architectural Exploration; System Verification and Validation

During today's keynote, Ghazi explained that as AI becomes pervasive, software plays a much larger role in semiconductor design, demanding a holistic systems approach to silicon innovation. From large, monolithic SoCs for AI workloads to new multi-die systems, the complexity and software-defined nature of today's designs requires verification systems with higher performance and greater capacity. In this context, Synopsys unveiled two new hardware-assisted verification (HAV) solutions for faster, higher capacity emulation and prototyping.

- Synopsys ZeBu® EP2 is the latest version in the Synopsys ZeBu EP family of unified emulation and prototyping systems. Available now, the new system provides the fastest emulation and prototyping platform for AI workloads, making it ideal for software bring-up, software/hardware validation, and power/performance analysis.
- Synopsys HAPS®-100 12 system is Synopsys' highest capacity and density FPGA-based prototyping system, with a mix of fixed and flexible interconnects and a rack-friendly design, particularly useful for prototyping big designs that require many FPGAs, such as multi-die systems and large SoCs. Available now, this new prototyping system shares a common hardware platform with Synopsys ZeBu EP2.

Together, these new offerings expand the industry's broadest HAV portfolio, helping customers reduce design risks and ensure that increasingly complex semiconductor designs perform as intended.

Announcing Synopsys Cloud Hybrid Solution for Seamless Bursting and Enhanced Engineering Productivity

The company today unveiled Synopsys Cloud Hybrid solution, which addresses a significant hurdle for mid-large semiconductor customers that have on-prem data centers but are sometimes limited by capacity and constrained on time. The new hybrid cloud solution enables these customers to seamlessly and efficiently burst from on-prem data centers to the cloud during peak needs.

In addition, it takes significant manual effort to designate certain blocks for on-prem resources and the cloud, plus additional time to transfer relevant design data and sync the data sets for processing. Synopsys Cloud Hybrid automatically splits the job based on available capacity and provides automated real-time data synchronization between a customer's cloud environment and on-prem data center. The solution eliminates the need for time-consuming, manual data transfers, helping customers maximize engineering productivity and accelerate time to results.

Synopsys Cloud Hybrid Solution is available to early access customers with a Synopsys Cloud contract.

Expanding Silicon IP Portfolio with Acquisition of Intrinsic ID

In a related announcement today, Synopsys completed the acquisition of Intrinsic ID, a leading provider of physical unclonable function (PUF) IP used in SoC design. The acquisition adds production-proven PUF IP to Synopsys' broadly used semiconductor IP portfolio, enabling chip designers to protect their SoCs by generating a unique on-chip identifier utilizing the inherent and distinctive characteristics of every silicon chip.

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The company plans to discuss its growing design IP business during this afternoon's investor meeting, which is co-located with SNUG Silicon Valley.

Virtual Access to SNUG Silicon Valley and Synopsys Investor Meeting

Happening March 20 and 21 in Santa Clara, Calif., SNUG Silicon Valley gathers the global Synopsys design community to discuss technology advancements, challenges, strategic collaborations, and business opportunities. Keynote presentations will be livestreamed and available for replay in the SNUG Newsroom. At 9:15a.m. PT on Thursday, March 21, Microsoft CVP Saurabh Dighe will deliver a keynote, "From Momentum to Scale: Unlocking Value in Innovation for the AI Transformation."

Today, Synopsys is also hosting a meeting with the investor community. Ghazi and CFOShelagh Glaser, along with key business executives, will discuss the company's silicon to systems strategy, progress, and growth opportunities. Synopsys Investor Day will begin after market close at 1:15p.m. PT. Investors and other interested parties may register for the webcast by

visiting the events section on Synopsys' investor website. A replay and summary materials from the presentations will also be available on the website following the event.

About Synopsys
Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements, including, but not limited to, statements regarding strategies related to our products, technology and services; business and market outlook, opportunities, strategies and technological trends, such as artificial intelligence; customer demand and market expansion; our planned product releases and capabilities; industry growth rates; and the expected benefits of our acquisition of Intrinsic ID. These statements involve risks, uncertainties and other factors that could cause our actual results, time frames or achievements to differ materially from those expressed or implied in such forward-looking statements. Such risks, uncertainties and factors include, but are not limited to: macroeconomic conditions and geopolitical uncertainty in the global economy; uncertainty in the growth of the semiconductor and electronics industries; the highly competitive industry we operate in; actions by the U.S. or foreign governments, such as the imposition of additional export restrictions or tariffs; consolidation among our customers and our dependence on a relatively small number of large customers; risks and compliance obligations relating to the global nature of our operations; and more. Additional information on potential risks, uncertainties and other factors that could affect Synopsys' results is included in filings we make with the SEC from time to time, including in the sections entitled "Risk Factors" in our latest Annual Report on Form 10-K and in our latest Quarterly Report on Form 10-Q. The information provided herein is as of March 20, 2024. Synopsys undertakes no duty to, and does not intend to, update any forward-looking statement, whether as a result of new information, future events or otherwise, unless required by law.

EDITORIAL CONTACT:
Kelli Wheeler
Synopsys, Inc.
650-584-5000
corp-pr@synopsys.com

SOURCE Synopsys, Inc.

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