Synopsys and Intel Foundry Accelerate Advanced Chip Designs with Synopsys IP and Certified EDA Flows for Intel 18A Process

Close Collaboration with EDA Flows and Broad IP Portfolio Enables Chipmakers to Boost Performance and Speed Time to Market

Highlights:

- Synopsys digital and analog EDA flows are certified and optimized to meet power, performance, and area targets on the Intel 18A process
- Broad portfolio of high-quality Synopsys IP reduces integration risk and accelerates time to market, providing a competitive edge to designers adopting the Intel 18A process
- Synopsys 3DIC Compiler, a unified exploration-to-signoff platform, enables multi-die system designs using Intel 18A and EMIB technologies

SUNNYVALE, Calif., Feb. 21, 2024 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced its AI-driven digital and analog design flows are certified by Intel Foundry for the Intel 18A process. In addition, through integration of high-quality Synopsys Foundation IP and Interface IP tuned for Intel Foundry technology, mutual customers can confidently design and deliver differentiated chips using advanced Intel Foundry technologies. With its certified EDA flows, multi-die system solution, and comprehensive IP portfolio in development for the Intel 18A process, Synopsys is helping designers accelerate the development of advanced high-performance designs. Today's announcement is being made at the Intel Foundry Direct Connect 2024 event, where Aart de Geus, Synopsys executive chair and founder, will present "Catalyzing SysMoore Together."

"The era of pervasive intelligence is driving significant silicon proliferation in the semiconductor industry, requiring strong ecosystem collaboration to help ensure customer success," said Shankar Krishnamoorthy, GM of the Synopsys EDA Group. "The AI-driven certified flows combined with the development of a broad Synopsys IP portfolio on the Intel 18A process, marks a significant milestone in our collaboration with Intel to help our mutual customers bring to life innovative devices, whether on the smallest processes or at angstrom scale."

"Our longstanding, strategic collaboration with Synopsys provides designers with access to industry-leading certified EDA flows and IP that deliver the best performance, power, and area for the Intel 18A technology," said Rahul Goyal, Vice President and General Manager, Product and Design Ecosystem, Intel Foundry. "This milestone in our collaboration enables mutual customers to boost productivity with EDA flows, achieve the highest utilization, and accelerate development of their advanced designs on the Intel Foundry process."

Power and Performance Gains with Backside Routing
Synopsys is working closely with Intel Foundry to enhance its EDA digital and analog design flows to help accelerate quality of results and time to results, while optimizing Synopsys IP and EDA flows for power and area on the Intel 18A process to take advantage of Intel's PowerVIA backside routing and RibbonFET transistors. The Intel 18A process technology is optimized using Synopsys design technology co-optimization tools to provide enhanced power, performance, and area. In addition, Synopsys Analog QuickStart Kit (QSK) and Synopsys Custom Compiler process design kit (PDK) for Intel 18A deliver proven methodologies for higher quality design and fast turnaround times.

To realize the advantages of the Intel 18A process and to bring differentiated products to market, Intel Foundry customers can integrate a comprehensive Synopsys IP portfolio built for Intel advanced process technologies. Synopsys will enable a range of its industry-leading interface and foundation IP to accelerate design execution and time to market for SoCs.

Synopsys and Intel Foundry are also driving multi-die systems forward with Synopsys 3DIC Compiler platform and Intel's advanced foundry processes. The platform addresses Intel Foundry chip designers' most complex multi-die system needs and provides automated routing for UCIe interfaces, while allowing seamless co-design of Intel's EMIB packaging technology. The Synopsys Multi-Die System Solution enables early architecture exploration, rapid software development and system validation, efficient die and package co-design, robust and secure die-to-die connectivity, and enhanced manufacturing and reliability.

Availability and Resources
The Synopsys Digital Design Family and Synopsys Custom Design Family tools are available now for advanced Intel Foundry processes. In addition, a broad portfolio of Synopsys IP for Intel 18A is in development.

- Learn more about the Synopsys Digital Design Family: https://www.synopsys.com/implementation-and-

signoff/fusion-design-platform.html
- Learn more about the Synopsys Custom Design Family: https://www.synopsys.com/implementation-and-signoff/custom-design-platform.html
- Learn more about Synopsys IP: https://www.synopsys.com/designware-ip.html
- Learn more about the Synopsys Multi-Die System Solution: https://www.synopsys.com/multi-die-system.html

About Synopsys
Catalyzing the era of pervasive intelligence, Synopsys, Inc. (Nasdaq: SNPS) delivers trusted and comprehensive silicon to systems design solutions, from electronic design automation to silicon IP and system verification and validation. We partner closely with semiconductor and systems customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Learn more at www.synopsys.com.

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