Synopsys and TSMC Streamline Multi-Die System Complexity with Unified Exploration-to-Signoff Platform and Proven UCIe IP on TSMC N3E Process

Comprehensive Multi-Die System Design Solution Supports 3Dblox 2.0 Standard and TSMC 3DFabric™ Technologies to Boost Productivity for Fast Heterogeneous Integration

Highlights:

- Synopsys 3DIC Compiler integrates with 3Dblox 2.0 standard for heterogeneous integration and a complete exploration-to-signoff solution.
- Synopsys UCIe PHY IP, which achieved first-pass silicon success on TSMC N3E process, provides low-latency, low-power, and high-bandwidth die-to-die connectivity.
- The combination of UCIe PHY IP and 3DIC Compiler optimizes multi-die system design for higher quality-of-results with minimal integration risk.

SUNNYVALE, Calif., Sept. 27, 2023 /PRNewswire/ – Synopsys, Inc. (Nasdaq: SNPS) today announced it is extending its collaboration with TSMC to advance multi-die system designs with a comprehensive solution supporting the latest 3Dblox 2.0 standard and TSMC's 3DFabric™ technologies. The Synopsys Multi-Die System solution includes 3DIC Compiler, a unified exploration-to-signoff platform that delivers the highest levels of design efficiency for capacity and performance. In addition, Synopsys has achieved first-pass silicon success of its Universal Chiplet Interconnect Express (UCIe) IP on TSMC's leading N3E process for seamless die-to-die connectivity.

"TSMC has been working closely with Synopsys to deliver differentiated solutions that address designers' most complex challenges from early architecture to manufacturing," said Dan Kochpatcharin, head of the Design Infrastructure Management Division at TSMC. "Our long history of collaboration with Synopsys benefits our mutual customers with optimized solutions for performance and power efficiency to help them address multi-die system design requirements for high-performance computing, data center, and automotive applications."

"Through our strong alliance with TSMC, we provide a comprehensive and scalable solution for unprecedented performance and efficiency in multi-die system designs." said Sanjay Bali, vice president of Strategy and Product Management for the EDA Group at Synopsys. "The ability to explore, analyze, and signoff multi-die system designs in a unified platform using a common standard like 3Dblox 2.0, along with the silicon proof of the Synopsys UCIe PHY IP on the TSMC N3E process, enables customers to accelerate system design from early architecture all the way to manufacturing."

Synopsys 3DIC Compiler, certified by TSMC, enables full-stack designs using the 3Dblox 2.0 standard and 3DFabric technologies in a unified die/package exploration, co-design, and analysis platform. Its integrated system analysis capability allows co-optimization of thermal and power integrity aligned with 3Dblox 2.0 system prototyping, which helps to ensure design feasibility. Synopsys and Ansys continue to collaborate and deliver signoff accuracy for system-level effects with the integration of Synopsys 3DIC Compiler and Ansys multi-physics analysis technologies. Synopsys 3DIC Compiler also interoperates with the Synopsys Test products to ensure volume test and quality.

Adopted by multiple leading companies, Synopsys' UCIe PHY IP on the TSMC N3E process has achieved first-pass silicon success, helping designers efficiently integrate the de facto standard for die-to-die connectivity into their multi-die systems. The results demonstrate maximum power efficiency and performance at 16Gbps, scalable to 24Gbps, with robust link margins. Supporting standard and advanced packaging, Synopsys' complete UCIe controller, PHY and verification IP solution offers test, repair, and monitoring capabilities to help ensure multi-die system reliability even during in-field operation. In addition, Synopsys provides a complete IP solution for HBM3 to address the high memory bandwidth requirements of multi-die systems. The combination of Synopsys IP and Synopsys 3DIC Compiler enables higher productivity and lowers IP integration risk by automating routing, interposer studies, and signal integrity analysis in support of the 3Dblox 2.0 die-to-die feasibility studies.

Availability

- Synopsys UCIe PHY IP on the TSMC N3E process and 3DIC Compiler are available now.
- Synopsys HBM3 IP is available on advanced TSMC processes.

Additional Resources

- Web: Synopsys Multi-Die System solution

- Synopsys Industry Insight Report: How Quickly Will Multi-Die Systems Change Semiconductor Design?
- Webinars: Requirements for Multi-Die System Success
- Web: Industry’s Broadest IP Portfolio for TSMC N3E Achieves First-Pass Silicon Success

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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