Synopsys Accelerates Advanced Chip Design with First-Pass Silicon Success of IP Portfolio on TSMC 3nm Process

Industry's Broadest IP Portfolio on TSMC N3E Yields Exceptional Power, Performance and Area for AI, Mobile and HPC

Highlights:

- Synopsys IP on TSMC N3E process delivers a competitive edge for chipmakers looking to reduce integration risk and accelerate time to first-pass silicon success
- Standards-compliant Synopsys Interface IP, including 112G Ethernet, LPDDR5X, DDR5, PCIe, USB/DisplayPort and MIPI C/D-PHY, enables wide interoperability
- Broad IP portfolio on TSMC's N3E process complements Synopsys' certified digital and custom design solutions to boost performance and minimize power consumption

SUNNYVALE, Calif., July 20, 2023 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) technology is unleashing a new wave of advanced designs with the industry's broadest portfolio of interface IP for the TSMC N3E process. Silicon success of Synopsys IP across multiple product lines, including the most widely used protocols, delivers leading power, performance, area (PPA) and latency. Synopsys' IP for the TSMC N3E node offers a fast path to TSMC N3P integration and enables chip designers to accelerate development of their AI, high-performance computing (HPC) and mobile designs.

"Synopsys provides a broad portfolio of high-quality IP that helps designers achieve their design goals and quickly integrate the necessary IP into their designs with less risk," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "Synopsys IP for TSMC's 3nm process has been adopted by dozens of leading companies to accelerate their development time, quickly achieve silicon success and speed their time to market."

"Our longstanding collaboration with Synopsys enables our mutual customers to benefit from a broad portfolio of IP that has been proven on TSMC's advanced process technologies," said Dan Kochpatcharin, head of the Design Infrastructure Management Division at TSMC. "The silicon success of Synopsys IP on TSMC's N3E process underscores our collective efforts to help designers address the stringent PPA and latency requirements of their SoC designs and accelerate silicon innovation for the next-generation AI, HPC and mobile applications."

Additional Resources

- Minimize Design Risk and Achieve First-Pass Silicon Success on TSMC's N3E Process
- Synopsys Advances Designs on TSMC N3E Process with Production-Proven EDA Flows and Broadest IP Portfolio for AI, Mobile and HPC Applications
- UCIe PHY IP Tape-Out on TSMC N3E Process

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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