Synopsys and TSMC Collaborate to Jumpstart Designs on TSMC's N2 Process with Optimized EDA Flows

Adopted by Leading Companies, the Synopsys Digital and Custom Design Flows Boost Performance and Minimize Power Consumption for Advanced SoCs on N3E and N2

MOUNTAIN VIEW, Calif., April 25, 2023 /PRNewswire/ -- In a continuing effort to meet stringent design targets for next-generation system-on-chips (SoCs) Synopsys, Inc. (Nasdaq: SNPS) today announced a collaboration with TSMC to deliver digital and custom design EDA flows on TSMC's most advanced N2 process. The TSMC N2 process leverages nanosheet transistors to offer up to 15% speed improvement at the same power or 30% power reduction at the same speed when compared with the TSMC N3E process, all while increasing chip density. This significant investment by Synopsys across the full EDA stack allows designers to jumpstart their N2 designs, differentiate their SoCs and accelerate their time to market.

"TSMC and Synopsys help our mutual customers achieve the best-in-class design results across the full Synopsys EDA stack on TSMC's most advanced N2 process," said Dan Kochpatcharin, head of Design Infrastructure Management Division at TSMC. "Our long-standing collaboration has helped innovators meet or exceed their design targets for the most demanding products across a wide range of applications, including high-performance computing, mobile and AI."

"Synopsys and TSMC continue to advance semiconductor technology, pushing the edge of design physics on the latest N2 process," said Sanjay Bali, vice president of Strategy and Product Management for the EDA Group at Synopsys. "Synopsys digital and custom design flows on TSMC's N2 process allows designers to significantly benefit from the advanced features of TSMC's N2 process and accelerate time to market."

The collaboration on N2 builds on the success of Synopsys certified EDA and IP solutions for the TSMC 3nm process technology, with several dozen successful tape-outs to date from leading companies. Synopsys customers can rely on the certified digital and custom design flows, Synopsys Foundation and Interface IP and the Synopsys Silicon Lifecycle Management (SLM) in-chip process, voltage and temperature (PVT) monitor IP to boost their N3 designs. Designers migrating their N4 and N5 designs to N3E can use the Synopsys EDA analog migration flow to efficiently reuse designs from one process node to another.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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