

Synopsys Advances Designs on TSMC N3E Process with Production-Proven EDA Flows and Broadest IP Portfolio for AI, Mobile and HPC Applications

Multiple Successful Tapeouts from Leading Companies Demonstrate Robustness of Synopsys Solutions for a Faster Path to Silicon Success

MOUNTAIN VIEW, Calif., Oct. 24, 2022 /PRNewswire/ -- Building on a long-standing collaboration with TSMC to drive continued innovation on advanced process nodes, [Synopsys, Inc.](#) (Nasdaq: [SNPS](#)) today announced several key achievements on the TSMC N3E process technology. The Synopsys production-proven digital and custom design flows have achieved certification on the TSMC N3E process. In addition, the flows and Synopsys' broad Foundation and Interface IP portfolio have achieved multiple successful tapeouts on the TSMC N3E process, helping customers accelerate silicon success. The collaborative efforts on the advanced process technology also extend to analog design migration, AI-driven designs and physical verification scaling in the cloud.

"TSMC's and Synopsys' long history of collaboration to advance semiconductor innovation addresses the increasingly complex challenges of emerging applications," said Dan Kochpatcharin, Head of Design Infrastructure Management Division at TSMC. "Synopsys' latest achievements in EDA and IP on the TSMC N3E process technology provide our mutual customers with robust solutions that help them meet the stringent power, performance and area targets for their innovative designs."

"These recent achievements mark another significant milestone of the continuous, successful collaboration between Synopsys and TSMC," said Sanjay Bali, vice president of Marketing and Strategy for the EDA Group at Synopsys. "Our substantial investment in providing certified EDA solutions and a silicon-proven IP portfolio for TSMC's most advanced processes gives designers a low-risk path to achieving their critical design requirements."

TSMC's N3E process extends its 3nm family with enhanced power, performance and yield, meeting the demands of workload-intensive applications like high-performance computing, AI and mobile. A joint effort on AI-driven design enablement with [Synopsys DSO.ai™](#) technology and [Synopsys Fusion Compiler](#) has resulted in multiple validated N3E test cases with better PPA and faster design closure. Aside from the IP readiness and certified flows, Synopsys is working closely with TSMC to scale physical verification in the cloud, using the [Synopsys IC Validator](#) product for N3E on the [Synopsys Cloud](#) software-as-a-service offering. The effort highlights how access to unlimited CPU capacity in the cloud delivers faster physical verification iterations. The two companies are also enabling customers to seamlessly transition existing designs on earlier process nodes to the TSMC N3E process.

Learn more by visiting these pages:

- Synopsys Digital Design Family: <https://www.synopsys.com/implementation-and-signoff/fusion-design-platform.html>
- Synopsys Custom Design Family: <https://www.synopsys.com/implementation-and-signoff/custom-design-platform.html>
- Synopsys Foundation IP: <https://www.synopsys.com/designware-ip/memories-logic-libraries.html>
- Synopsys Interface IP: <https://www.synopsys.com/designware-ip/interface-ip.html>

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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