Synopsys Unveils Breakthrough Golden Signoff ECO Solution, Delivering 10x Productivity Improvement

Solution Delivers Fastest Path to Chip Design Closure for HPC, AI, Automotive and Mobile Designs on Advanced Process Technologies

MOUNTAIN VIEW, Calif., Oct. 5, 2022 /PRNewswire/ -- To boost productivity and enhance power, performance and area (PPA) of advanced electronic designs, Synopsys, Inc. (Nasdaq: SNPS) today announced the breakthrough golden signoff ECO solution that addresses lengthy engineering design closure times. The Synopsys PrimeClosure solution combines Synopsys' leading engineering change order (ECO) signoff solutions, Synopsys PrimeECO™ and Synopsys Tweaker™ ECO, with breakthrough innovations, delivering the fastest ECO closure times with high capacity and golden Synopsys PrimeTime® signoff accuracy. Early customers have achieved up to 45% better timing, up to 10% better power, up to 50% fewer ECO iterations and up to 10x higher design productivity compared to traditional ECO flows.

"Given our focus on large-scale, advanced-node designs in areas such as automotive, data centers, networking and smart devices, fast turnaround time on ECOs is essential to our business success," said Kenta Sokawa, general manager, Back End Development Division, Global Development Group at Socionext. "The Synopsys PrimeClosure solution reduced our turnaround time by over 5x, used 3x less machine memory and required 5x fewer machine resources. The early results are impressive, and we are excited to collaborate with Synopsys to push the envelope on conventional ECO challenges with the aim of achieving over 10x design closure productivity improvement for our large designs."

The Synopsys PrimeClosure solution is available to early adopters now with general availability targeted for December 2022. For more information, visit: https://www.synopsys.com/implementation-and-signoff/signoff/primeclosure.html.

Accelerating Design Convergence

Application areas like data centers, mobile, automotive, AI and IoT are demanding aggressive PPA targets. Advanced process nodes bring new physical rules and introduce new effects which impact PPA. The enormous size and complexity of deep-submicron designs means that every analysis and ECO optimization run to fix issues takes longer and consumes more compute resources. Handling this large number of violations and driving convergence to reduce it to zero is a big part of the ECO challenge.

The Synopsys PrimeClosure solution, with its innovative surgical optimization feature, improves design metrics like PPA, timing, clock network, voltage drop, variation and aging. The solution is tightly integrated with Synopsys Fusion Compiler™ RTL-to-GDSII solution and Synopsys PrimeTime static timing analysis solution for golden signoff accuracy, delivering a full flow that accelerates design convergence and time-to-market of large designs.

With its novel gigachip hierarchical technology, the Synopsys PrimeClosure solution seamlessly scales designs with billion+ instances and hundreds of scenarios with a relatively small number of machines to deliver the industry's fastest turnaround time (TAT). Its optimized pruning technology efficiently sifts through thousands of scenarios and hundreds of hierarchical blocks to reduce the number of datasets for optimization, resulting in TAT speedup by over 40% and reduced memory by up to 60%.

Optimizing Last-Mile Advanced Chip Design Closure

Last-mile design optimization is critical to achieve optimal PPA. The Synopsys PrimeClosure solution has direct access to incrementally enabled placement, routing, extraction, physical verification, equivalence checking and signoff technologies from the market-leading Synopsys Digital Design Family. The Synopsys PrimeClosure solution is integrated with Ansys RedHawk-SC digital power integrity signoff solution, enabling a breakthrough automated late-stage golden signoff timing-aware ECO solution to accurately account for and fix up to 50% of late-stage dynamic voltage drop violations and maximize energy efficiency without impacting chip timing. The single-environment design closure cockpit ensures every change is fully implemented and validated and creates new opportunities for placement, routing, and timing co-optimization to achieve PPA results previously impossible in traditional design closure flows.

"Scaling productivity in hyperconvergent designs requires innovative solutions that can quickly and efficiently optimize PPA targets in very large design spaces," said Jacob Avidan, senior vice president of Engineering for the Silicon Realization Group at Synopsys. "The Synopsys PrimeClosure product provides the industry with a breakthrough golden signoff ECO solution that enables designers to confidently achieve the fastest path to design closure, so companies can do more in significantly less time."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

SOURCE Synopsys, Inc.