Synopsys Delivers Higher Productivity and Quality for Advanced-Node 5G/6G SoCs on Samsung Foundry's Low-Power Process

Jointly Developed End-to-End RF Design Reference Flow and Design Solutions Kit, Integrated with Ansys Technologies, Speed Design Closure

MOUNTAIN VIEW, Calif., July 11, 2022 /PRNewswire/ -- Enabling mutual customers to accelerate their development of advanced-node RF designs for 5G/6G applications, Synopsys (Nasdaq: SNPS) today announced it has developed an RF design reference flow and companion design solutions kit (DSK) that enhance productivity and speed design closure on Samsung Foundry's 8nm RF low-power FinFET process. The 8nm RF design reference flow, which features tightly integrated solutions from Synopsys and Ansys, enhances time-to-results, quality-of-results and cost-of-results for next-generation RF design.

"Samsung's latest RF solution, the 8nm RF process technology, could massively improve the performance and power efficiency of 5G communication chips," said Sangyun Kim, corporate vice president of the Foundry Design Technology Team at Samsung Electronics. "We are pleased that the 8nm RF design reference flow and design solution kit that we developed in close collaboration with Ansys and Synopsys will support our mutual customers in meeting the demands of growing design complexity in today's hyper-connected world."

To learn more about Synopsys RF design solutions, visit:https://www.synopsys.com/rf-design.html.

Enabling Greater Connectivity in Our Digital World

Advanced-node analog and RF designs are integral to the applications fueling our digital world of smart everything. However, it can be complex and time-consuming to design these chips to meet the bandwidth and latency requirements of applications like 5G/6G, automotive and high-performance computing. Available today, the 8nm RF design reference flow streamlines the process with features that deliver faster layout design turnaround time with industry-leading circuit simulation and layout productivity performance, as well as accurate electromagnetic (EM) modeling. The reference flow documents a proven methodology for RF design with Synopsys and Ansys tools that spans schematic design, simulation, layout, extraction, electromagnetic (EM) simulation and physical verification. The associated DSK includes a set of application notes, tutorials and design examples that cover advanced design methodology topics, including:

- In-design parasitic analysis – the ability to measure parasitics on canvas using signoff tools during layout
- On-chip inductor design – the ability to generate inductor devices with Ansys VeloceRF™ integrated with Synopsys Custom Compiler™ design and layout environment
- Partial layout extraction and simulation – the ability to do parasitic simulation using parasitics extracted from partially completed designs to get early feedback of the parasitic impact on designs
- Design reuse with templates – the ability to create high-quality layout in less time by using Synopsys Custom Compiler layout templates

Key elements of the flow include theSynopsys Custom Design Family of products, featuring theSynopsys Custom Compiler™ design and layout product, Synopsys PrimeSim™ circuit simulation product, Synopsys StarRC™ parasitic extraction signoff product and Synopsys IC Validator™ physical verification product; Ansys VeloceRF inductive component and transmission line synthesis product; and Ansys RaptorX™ and Ansys RaptorH™, the advanced nanometer EM analysis products.

"Ansys is excited to collaborate with Synopsys and Samsung on an advanced reference flow for RF design," said Yorgos Koutsoyannopoulos, vice president of Research and Development at Ansys. "Working seamlessly with the Synopsys Custom Compiler design and PrimeSim simulation solutions, Ansys inductor design and EM extraction tools have the highest capacity to handle the most challenging designs as well as the ability to model all advanced process effects and enable a complete end-to-end RF design flow. Together, we're delivering an intuitive and easy-to-use flow for the design, optimization and verification of RF design blocks."

"Synopsys and Samsung have a history of working closely together to enable our mutual customers to achieve smooth and productive design workflows for the latest Samsung technologies," said Aveek Sarkar, vice president of Engineering at Synopsys. "Tapping into our close ties with Ansys, this new RF design reference flow and DSK streamlines the process for developing the advanced wireless systems that will continue to drive our smart everything world."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic

products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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