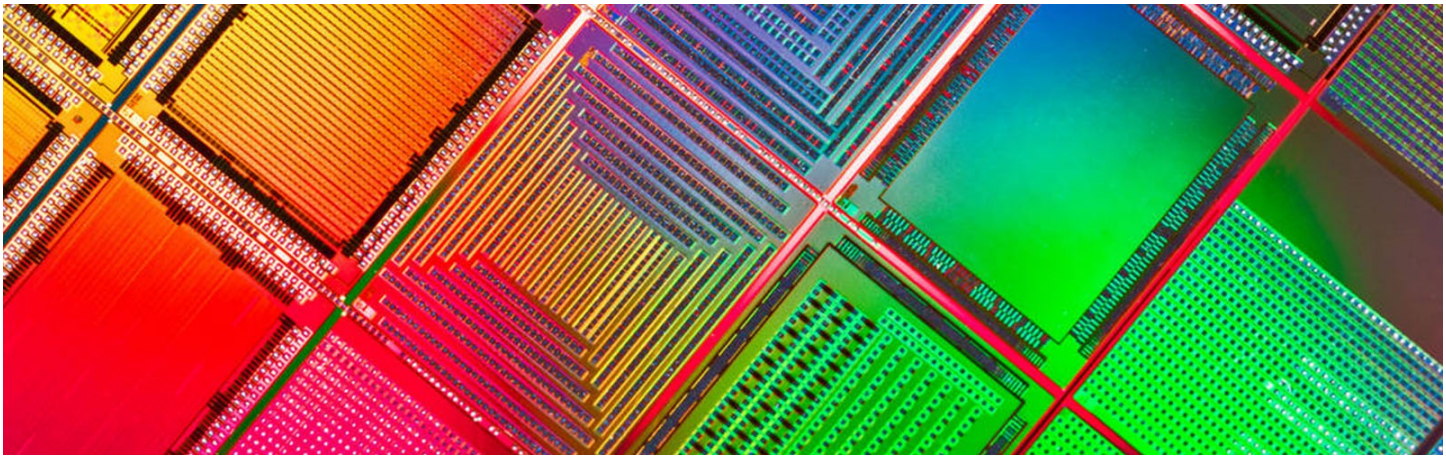
Synopsys Drives Chip Innovation for Next-Generation Mobile and HPC Designs on TSMC N3E and N4P Processes



Synopsys Digital and Custom Design Flows Certified for TSMC N3E and N4P Processes and Broad Synopsys IP Portfolio Available Now

MOUNTAIN VIEW, Calif., June 13, 2022 /PRNewswire/ -- Helping customers optimize performance, power and area (PPA) for next-generation system-on-chips (SoCs) used in demanding mobile and high-performance computing applications, Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified the Synopsys digital and custom design flows for its industry-leading N3E and N4P process technologies. In addition, Synopsys' leading Foundation IP and Interface IP are available now on the TSMC N3E and N4P processes to accelerate SoC development and minimize design risk. Adopted by leading customers, the digital and custom design flows and IP are based on the latest versions of TSMC's design rule manual (DRM) and process design kits (PDKs).

"TSMC and Synopsys have successfully collaborated for decades, with the shared goal of helping our mutual customers meet the aggressive PPA demands of increasingly complex SoCs," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "By enabling Synopsys' design solutions on TSMC's high-performing and power-efficient N3E and N4P processes, customers can produce innovative, advanced chips for a variety of demanding, compute-intensive applications."

Learn more about Synopsys digital and custom flows, as well as Synopsys Foundation IP and Synopsys Interface IP.

The integrated Synopsys Custom Design Family features new innovations in synthesis, place-and-route, physical verification and timing signoff, which enables the best possible PPA results and faster design closure. On the custom side, Synopsys Custom Compiler™ design and layout product, part of the Synopsys Custom Design Family and successfully validated by the Synopsys IP team, features enhancements that strengthen productivity for designers using TSMC's N3E process. In addition, the Synopsys PrimeSim™ circuit simulation technology delivers required accuracy for advanced-node designs, providing signoff coverage for circuit simulation and reliability requirements.

"Our deep history of collaboration with TSMC through every process generation has enabled Synopsys to co-optimize our digital and custom design families and IP portfolio to provide compelling PPA advantages for our mutual customers," said Sanjay Bali, vice president of marketing and strategy for the Silicon Realization Group at Synopsys. "We are seeing first-hand how companies are achieving successful designs and delivering the next level of innovation with Synopsys EDA flows and IP on TSMC's advanced N3E and N4P processes."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at https://www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

SOURCE Synopsys, Inc.