Samsung Foundry Adopts Leading Voltage-Timing Signoff Solution from Synopsys and Ansys for Advanced-Node, Energy-Efficient Chips

Long-Standing Partnership Delivers Highly Integrated Technology that Provides Strong Silicon Correlation and Prevents Costly Timing Failures

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Highlights from this announcement:

- Jointly developed solution, built on industry golden Synopsys PrimeTime signoff technology and Ansys RedHawk-SC, prevents dynamic voltage-drop- (DVD-) induced failures and minimizes timing pessimism
- Solution is the latest in a long-standing partnership between Synopsys and Ansys, resulting in highly integrated technologies that enhance design optimization
- Samsung Foundry has achieved high silicon correlation with the solution

Synopsys, Inc. (Nasdaq: SNPS) today announced that an advanced voltage-timing signoff solution developed in collaboration with Ansys has been adopted by Samsung Foundry to accelerate the development of its energy efficient designs with optimal power, performance and area (PPA). The offering is built on golden-signoff products, including the Synopsys PrimeTime® static timing analysis, Synopsys PrimeShield™ design robustness, Synopsys Tweaker™ ECO and Ansys® RedHawk-SC™ digital power integrity signoff solutions, and delivers the industry's highest accuracy and throughput, savings weeks of time.

Samsung Foundry has reported high silicon correlation using the integrated solution. "Dynamic voltage-drop and power integrity are significant challenges for energy efficient design," said Sangyun Kim, vice president of Design Technology at Samsung Foundry. "The new Synopsys-Ansys voltage-timing solution shows good correlation with silicon and is especially effective in accurately estimating DVD impact on bus-pipeline paths. Samsung Foundry plans to deploy the solution on production designs at advanced nodes to prevent failures in silicon and maximize design energy efficiency."

At advanced nodes, DVD and power integrity become even more challenging, with the potential for increased variability and greater difficulties in achieving accurate delay calculations. However, inaccurate timing assessment of DVD violations can result in missed DVD-related timing silicon failures. Some design teams utilize pessimistic guard-bands and margins as a work-around, but this approach can lead to over-design, sub-optimal energy efficiency and PPA, as well as protracted design closure iterations. The new solution catches real design and silicon bugs that traditional, disjointed flows can miss, preventing over-fixing by minimizing DVD and timing pessimism.

"Building on our long-standing collaboration to enhance design implementation, we're pleased to extend our efforts to the signoff realm," said John Lee, vice president and general manager of the Electronics and Semiconductor Business Unit at Ansys. "With our RedHawk-SC technology along with PrimeTime static timing analysis solution, Ansys and Synopsys are the only two companies that can address signoff fidelity, silicon correlation and throughput at advanced nodes, accelerating time-to-market and quality-of-results."

The PrimeTime and PrimeShield solutions identify DVD-sensitive critical paths, sharing this data with RedHawk-SC, which generates critical path-aware directed scenarios and vectors to perform accurate DVD analysis. The RedHawk-SC solution also provides high-fidelity, instance-specific piecewise-linear VDD and VSS waveforms to the PrimeTime solution, which employs its advanced waveform propagation engine to compute highly accurate timing impact insights.

"Working closely with Ansys, we've solved one of the industry's toughest timing signoff-related challenges, enabling designers to reduce iterations and achieve their energy-efficiency and PPA targets weeks earlier," said Shankar Krishnamoorthy, general manager and corporate staff for the Silicon Realization Group at Synopsys. "Our PrimeTime solution has demonstrated 3% correlation to HSPICE, the most accurate in the industry, while the cloud-based architecture of RedHawk-SC delivers the speed and capacity for full-chip analysis. From our earlier work integrating RedHawk Analysis Fusion with our IC Compiler™ II place and route solution and Fusion Compiler™ RTL-to-GDSII solutions, we're continuing to empower designers to meet their tough power integrity requirements and realize better PPA outcomes."

Learn more about PrimeTime static timing analysis, PrimeShield design robustness and Tweaker ECO solutions, all part of the Fusion Design Platform™. Learn more about Ansys RedHawk-SC.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

Editorial Contact:

Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

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