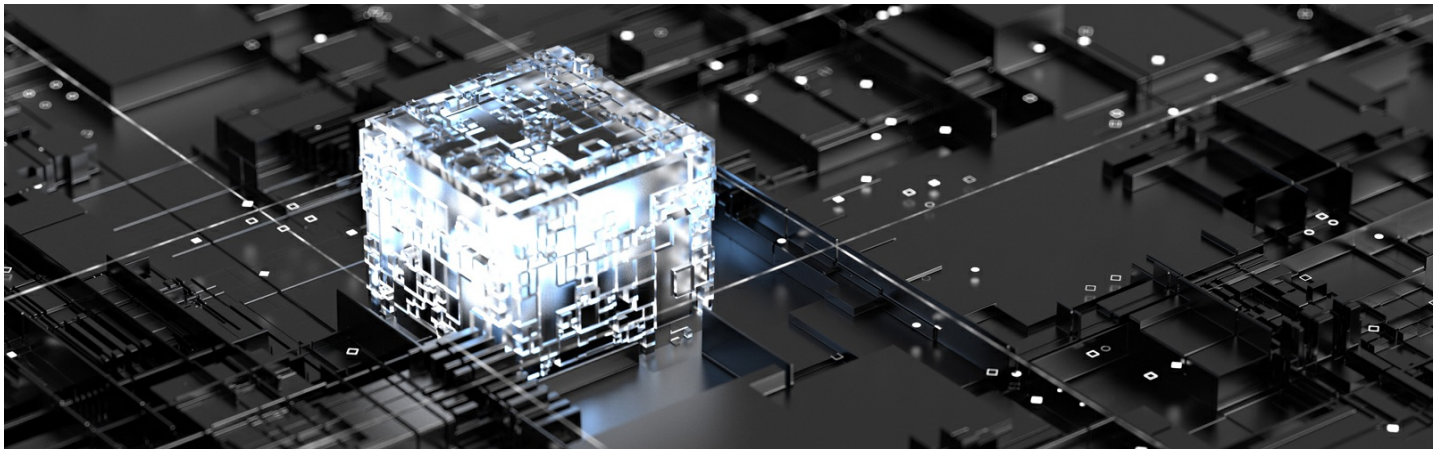
Synopsys Extends Industry Leadership as Customers Surpass 500 Tapeouts Using Flagship Fusion Compiler Solution

Customers Detail Significant Gains Including 20% Better Performance, 15% Lower Power and 5% Smaller Area



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Highlights from this announcement:

- Tapeouts encompass 40nm to 3nm designs across a broad spectrum of market segments including 5G mobile, HPC, AI and hyperscale data centers
- Leading semiconductor companies highlight seamless deployment and gains achieved with Synopsys Fusion Compiler along with further advantages realized from utilizing the Synopsys Fusion Design Platform

Synopsys, Inc. (Nasdaq: SNPS) has extended its industry leadership in digital design implementation, today announcing that customers using its flagship Fusion Compiler™ RTL-to-GDSII solution have achieved more than 500 tapeouts since the solution's general availability in 2019. Customers who have taped-out their designs with Fusion Compiler span the 40nm to 3nm process nodes at leading semiconductor companies across high-growth market verticals, including high-performance computing (HPC), artificial intelligence (AI) and 5G mobile.

With a unified architecture and optimization engines that facilitate signoff-accurate performance, power and area (PPA) metrics while minimizing design iterations and late surprises, Fusion Compiler addresses significant challenges faced by today's designers in meeting stringent PPA goals, especially on advanced nodes under aggressive schedules. Customers have achieved, on average, up to 20% better performance, 15% lower power and 5% smaller area compared to competitive solutions.

"The seamless production deployment of Synopsys' Fusion Compiler solution has helped advance our leadership position by delivering superior quality-of-results, including significantly better utilization rates and accelerated time-to-market," said Ilyong Kim, vice president of Design Technology Team, System LSI Business, Samsung Electronics. "Its unique single-data model and unified engines, along with built-in signoff timing, parasitic extraction and power analysis that eliminate design iterations, sets Fusion Compiler

apart from other industry solutions. We have experienced the benefits of Fusion Compiler consistently through multiple, successful design tape-outs and are expanding its deployment, including the adoption of the latest machine learning technology to further our customer-centric differentiation."

"Kioxia Corporation is a leading memory supplier in a highly competitive semiconductor segment, with leadership positions in memory controllers with high performance-per-watt," said Kazunari Horikawa, senior manager of Design Technology Innovation Division at Kioxia Corporation. "Our partnership with Synopsys enabled a complete Fusion Compiler design flow and improved the flow efficiency significantly. In addition, the Synopsys Fusion Design Platform with Synopsys' TestMAX has enabled us to shift-left our design methodology and achieve up to 40% power reduction and 10% smaller area in our latest tape-out, further advancing our leadership position. We look forward to working with Synopsys for further productivity gains with Fusion Compiler."

Production-Proven, Scalable Unified Data Model for Predictable Quality of Results

As the industry's only single-data-model and golden-signoff-enabled RTL-to-GDSII implementation product, Fusion Compiler utilizes a highly scalable, unified data model and comprises an analysis backbone that leverages technology from the industry's golden-signoff analysis tools. Having all of these capabilities within a single, integrated shell delivers unique, customized flows for predictable quality of results (QoR) and signoff correlation. Additionally, its unique architecture is augmented by machine learning technologies throughout the flow, enabling new levels of productivity and QoR.

"Our customers face continuing pressure to deliver solutions into new markets on tight timelines. Fusion Compiler enables our customers to accelerate bringing their products to market while delivering the most differentiated PPA," said Sanjay Bali, vice president of Marketing and Strategy, Silicon Realization Group at Synopsys. "Seeing our customers realize more than 500 tapeouts using Fusion Compiler reaffirms the industry's need for a vertically integrated RTL-to-GDSII solution that delivers the best possible PPA."

Synopsys' Fusion Compiler digital design implementation solution is the centerpiece of the Synopsys Fusion Design Platform™, the industry's first AI-enhanced, cloud-ready design solution set that redefines conventional EDA tool boundaries across synthesis, place-and-route and signoff. The platform uses machine learning to speed up computation-intensive analysis, predicts outcomes to enhance decision-making and utilizes past learning to drive better results.

At the recent Synopsys Digital Design Technology Symposium event, customers such as AMD, Arm and MediaTek detailed their design experiences with Fusion Compiler and the Fusion Design Platform. The event is now available on-demand.

Learn more about Fusion Design Platform: https://www.synopsys.com/implementation-and-signoff/fusion-design-platform.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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