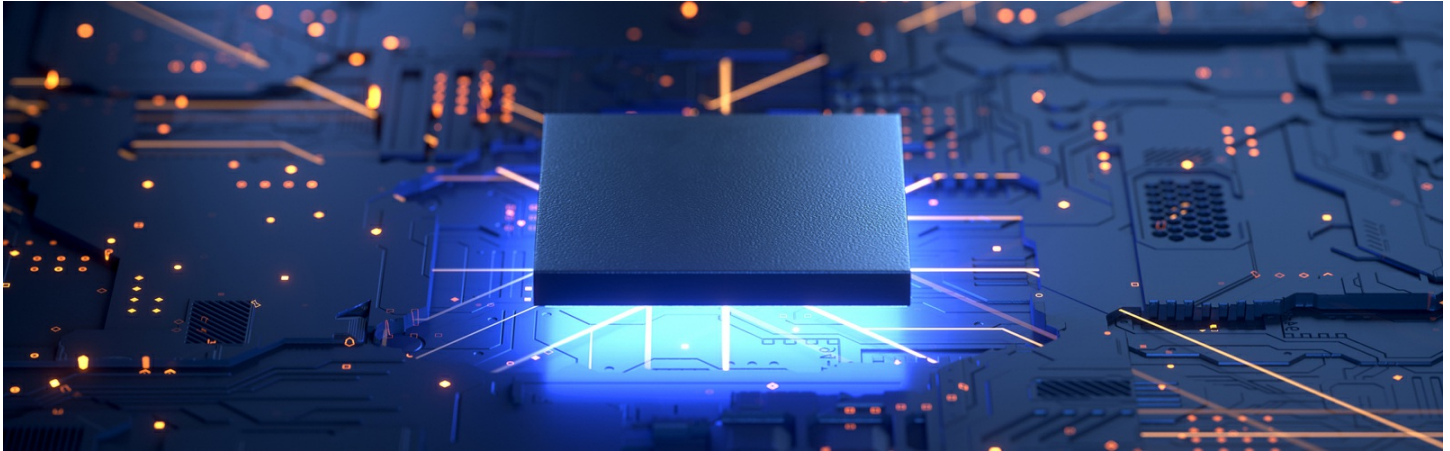# Synopsys Full EDA Flow First to Achieve Samsung Foundry 4LPP Process Certification

Digital and Custom Design Platforms, Along with High-Quality IP, Accelerate Customer Adoption While Minimizing Risk at New Node for HPC, AI, 5G and Other Advanced SoCs

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Highlights:

- Synopsys Fusion Design Platform and Custom Design Platform are first to achieve Samsung Foundry certification on 4LPP process, part of the foundry's comprehensive technology roadmap to help chipmakers design and deliver faster, more power-efficient chips
- Synopsys 3DIC Compiler has been validated for the Samsung Foundry Multi-Die Integration (MDI) flow, which incorporates the latest 4LPP process technology advances and provides scalability for hundreds of billions of transistors
- Synopsys DesignWare IP for 4LPP process delivers low latency, maximum power efficiency and high bandwidth while minimizing integration risks

Exemplifying a commitment toward accelerating the development of power-efficient, advanced-node chips, Synopsys, Inc. (Nasdaq: SNPS) today announced that its full EDA flow has been certified by Samsung Foundry for its new 4LPP (4nm Low Power Plus) process. The 4LPP process, which is available now, represents the latest implementation of Samsung Foundry's unique FinFET technology, which delivers chip density, performance and power advantages for SoCs fueling some of today's most in-demand applications, including high-performance computing, AI, and 5G infrastructure.

The Synopsys solutions certified for Samsung Foundry's 4LPP process encompass the full digital, analog and mixed-signal implementation and signoff flow. In addition, collaboration between the two companies has resulted in the availability of Synopsys 3DIC Compiler solution for the Samsung Foundry Multi-Die Integration (MDI™) flow, which is proven on 4LPP technology. 3DIC Compiler is a full exploration-to-signoff 3D solution to manage the complexity of hundreds of billions of transistors, while driving power, performance and area (PPA) per cubic mm silicon optimization. Synopsys is also developing a portfolio of DesignWare® Foundation IP and Interface IP that delivers low latency, high bandwidth and power efficiency for chips developed on the 4LPP process.

"Samsung Foundry is pleased to have worked closely with Synopsys to ensure readiness of its full EDA flow for our 4LPP process," said Sangyun Kim, vice president of Foundry Design Technology Team at Samsung Electronics. "Synopsys is an ideal partner to join forces on pathfinding efforts to facilitate new-node enablement as we further advance our roadmap on new technologies such as our upcoming 3nm gate-all-around process."

As the first EDA vendor to achieve full-flow certification for the 4LPP process via the SAFE-QEDA program, Synopsys is poised to accelerate a smooth adoption process for customers, minimizing risk and reducing turnaround time and costs. The SAFE-QEDA program is designed to mitigate risks of new node adoption.

"Our close collaboration continues to accelerate technology advances to drive innovation in high-performance computing, AI accelerators, AR/VR and other popular application areas," said Shankar Krishnamoorthy, GM and

corporate staff for the Silicon Realization Group at Synopsys. "The certification of our platforms for Samsung Foundry's 4LPP process ensures the highest level of silicon correlation and design robustness to enable chipmakers to realize best-in-class PPA and faster turnaround times."

Synopsys digital design solutions that are part of the certified flow are anchored by the Fusion Design Platform™, which, with its single data model and machine learning capabilities, spans the entire design-to-silicon lifecycle, accelerating development of innovative, hyper-convergent designs. The solutions in this flow include:

- Synopsys Fusion Compiler™ RTL-to-GDSII digital implementation solution
- Synopsys IC Compiler™ II place-and-route solution
- Synopsys 3DIC Compiler unified exploration-to-signoff 3D solution
- Synopsys Design Compiler® Graphical synthesis solution
- Synopsys Design Compiler NXT RTL synthesis solution
- Synopsys TestMAX DFT advanced design-for-test solution
- Synopsys TestMAX ATPG advanced pattern generation solution
- Synopsys StarRC™ golden signoff parasitic extraction solution
- Synopsys PrimeTime® static timing analysis solution
- Synopsys PrimePower RTL to signoff power analysis solution
- Synopsys IC Validator™ physical verification solution

Synopsys custom design solutions that are part of the certified flow are anchored by the Custom Design Platform, which includes PrimeSim™ Continuum simulation solution and provides a unified suite of design and verification tools for analog and mixed-signal designs. The PrimeSim Continuum solution includes PrimeSim HSPICE, PrimeSim SPICE, PrimeSim Pro and PrimeSim XA simulators. Other solutions in this flow include:

- Synopsys PrimeSim EMIR analysis solution for transistor-level power signoff
- Synopsys Custom Compiler™ design environment for full-custom analog, custom digital and mixed-signal ICs
- Synopsys SiliconSmart® cell, I/O and memory characterization solution
- Synopsys PrimeLib unified library characterization and validation solution

Synopsys is also developing a broad DesignWare IP portfolio for Samsung's 4LPP process, including:

- Synopsys Multi-Protocol 32G PHY IP, including PCI Express® 5.0 and 25G Ethernet
- Synopsys Embedded Memories, including TCAMs
- Synopsys Logic Libraries
- Synopsys General-Purpose I/O (GPIO)
- Synopsys High Performance Core (HPC) Design Kit

Samsung SAFE Forum 2021

Synopsys President and COO Sassine Ghazi will present a keynote talk at Samsung Advanced Foundry Ecosystem (SAFE™) Forum 2021 on November 17. The event will also feature numerous technical presentations from Synopsys experts. For more information, visit: https://www.synopsys.com/events/samsung-safe.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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