Synopsys and TSMC Drive Chip Innovation with Development of Broadest IP Portfolio on TSMC N4P Process

DesignWare Interface and Foundation IP Deliver Optimized Power and Performance for High-Performance Computing and Mobile SoCs

MOUNTAIN VIEW, Calif., Oct. 27, 2021 /PRNewswire/ --

Highlights from this announcement:

- DesignWare Interface IP for the most widely used protocols delivers the required high bandwidth and low latency for efficient data connectivity in compute-intensive designs on TSMC N4P process
- DesignWare Foundation IP offers high-speed, area-optimized and low-power embedded memories, logic libraries, GPIOs and TCAMs
- Broad IP portfolio on TSMC's N4P process complements Synopsys' certified digital and custom design solutions for the process, accelerating time to silicon success

To facilitate chip innovation and enable designers to quickly achieve silicon success of complex high-performance computing (HPC) and mobile SoCs, Synopsys, Inc. (Nasdaq: SNPS) today announced a collaboration with TSMC to develop a broad portfolio of Synopsys DesignWare® Interface and Foundation IP on the TSMC N4P process. The collaboration enables designers to access high-quality IP that aligns with their aggressive design and project schedule requirements on TSMC's most advanced process, while optimizing for performance, power, area, bandwidth and latency.

"We work closely with our Open Innovation Platform® (OIP) ecosystem partners to enable next-generation designs benefiting from the significant power and performance boost of our newest N4P process, which provides unique PPA balance to allow customers to continue to deliver leading HPC, mobile and other high performance products," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "TSMC's long-term collaboration with Synopsys continues to deliver high-quality DesignWare IP on TSMC's most advanced processes, allowing designers to fully realize the advantages of the N4P process and launch differentiated products quickly to the market."

"Developing DesignWare IP on TSMC N4P process gives designers confidence that they can quickly integrate the IP into their designs and benefit from the performance, power and area improvements of the N4P process technology," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "Our significant investment in developing silicon-proven and standards-compliant IP on the most advanced process technologies provides designers with a low-risk path to achieving their design requirements."

Synopsys' broad DesignWare IP portfolio includes logic libraries, embedded memories, IOs, PVT monitors, embedded test, analog IP, interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Our extensive investment in IP quality and comprehensive technical support enable designers to reduce integration risk and accelerate time-to-market. For more information, please visit https://www.synopsys.com/designware.

Product Availability and Resources

DesignWare Interface and Foundation IP portfolios on TSMC N4P process are scheduled to be available starting in Q1 of 2022.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454

simone@synopsys.com

SOURCE Synopsys, Inc.