Synopsys Expands Strategic Technology Collaboration with TSMC to Extend 3D-System Integration Solutions for Next-Generation High-Performance Computing Designs

Synopsys' 3DIC Compiler Delivers Seamless Access to TSMC 3DFabric Technologies

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Highlights of this Announcement:

- Expanded strategic collaboration delivers comprehensive 3D-system integration capabilities, enabling the aggregation of hundreds of billions of transistors in a single package
- Synopsys 3DIC Compiler, the unified, multi-die implementation platform, seamlessly integrates TSMC 3DFabric technologies-based design methodologies, to offer a complete exploration-to-signoff design platform
- This joint collaboration combines TSMC's technology advancements with the converged architecture, advanced in-design analysis framework and signoff tools of 3DIC Compiler to deliver the required performance, power and transistor-volume density

Synopsys, Inc. (Nasdaq: SNPS) today announced it has expanded its strategic technology collaboration with TSMC to deliver the next level in system integration to address the increasingly critical performance, power and area targets for high-performance computing (HPC) applications. By leveraging Synopsys' 3DIC Compiler platform, customers significantly advance high-capacity 3D system design through efficient access to TSMC 3DFabric™-based design methodologies. These methodologies deliver 3D chip-stacking support in the System-on-Integrated-Chips (TSMC-SoIC™) technology and 2.5/3D advanced packaging support in Integrated Fan-Out (InFO) and Chip-on-Wafer-on-Substrate (CoWoS®) technologies. The coalescence of support for these advanced methodologies in the 3DIC Compiler platform's highly integrated, multi-die design addresses the complete exploration-to-signoff challenge, driving the future realization of next-generation hyper-convergent 3D systems comprising hundreds of billions of transistors in a single package.

"TSMC works closely with our Open Innovation Platform® (OIP) ecosystem partners to enable the next wave of innovation in the HPC space," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "This joint effort combining Synopsys' 3DIC Compiler platform and TSMC's chip stacking and advanced packaging technologies will help our customers meet design requirements on power and performance and achieve success in leading-edge SoC designs for HPC applications."

The 3DIC Compiler platform is a complete, end-to-end solution for efficient 2.5/3D multi-die design and full system integration. Built on the Synopsys Fusion Design Platform™ common, single-data-model infrastructure, the 3DIC Compiler platform coalesces transformative, multi-die design capabilities and leverages Synopsys' world-class implementation and signoff technologies to offer a complete exploration-to-signoff platform – all in a single, consolidated 3DIC cockpit. This hyper-converged solution comprises 2D and 3D visualization, cross-hierarchy exploration and planning, design and implementation, design for test and full-system validation and signoff analysis.

"Delivering the substantial scaling necessary for the growing surge of AI-centric workloads and domain-optimized computing requires bold leadership and wide-ranging, collaboration-led innovation," said Shankar Krishnamoorthy, general manager and corporate staff for the Silicon Realization Group at Synopsys. "Our trailblazing work with TSMC on their latest 3DFabric technology enables the imagination and realization of previously unattainable levels of 3D system integration. This leap in achievable performance, power and transistor-volume density will both impact and help to shape numerous existing and emerging applications and markets, by leveraging the 3DIC Compiler platform and TSMC's highly accessible integration technologies."

The 3DIC Compiler platform delivers high levels of efficiency while also scaling in capacity and performance to bring seamless support for various heterogeneous process and stacked dies. By leveraging integrated signoff solutions, including the Synopsys PrimeTime® timing signoff solution, StarRC™ parasitic extraction signoff, Tweaker™ ECO closure solution and IC Validator™ physical verification solution coupled with the Ansys® RedHawk-SC Electrothermal™ family of multi-physics analysis solutions and testability with Synopsys TestMax DFT solution, 3DIC Compiler platform provides best-in-class co-analysis technologies for the fastest convergence to robust, high-performance designs.

Read more about the 3DIC Compiler platform:
https://www.synopsys.com/implementation-and-signoff/3dic-design.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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