Synopsys Digital and Custom Design Platforms Achieve Certification for TSMC N3 Process

The Platforms Optimize PPA for Next-Generation HPC, Mobile, 5G and AI Designs

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Highlights:

- Synopsys platforms deliver enhanced features to support new requirements for TSMC N3 and N4 processes
- The Synopsys Fusion Design Platform facilitates faster timing closure and full-flow correlation from synthesis through timing and physical signoff
- The Synopsys Custom Design Platform delivers improved productivity

In a continuing effort to optimize power, performance and area (PPA) for next-generation system-on-chips (SoCs), Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified the Synopsys digital and custom design platforms for TSMC's 3nm technology. The certification with rigorous validation, based on TSMC's latest version of the design rule manual (DRM) and process design kits (PDKs), is the result of a multi-year collaboration between the two companies. In addition to this certification, Synopsys' digital and custom design platforms have also been certified for TSMC's N4 process.

"We're pleased to see the results of our multi-year collaboration with Synopsys and the certification of their design platform solutions on TSMC's most advanced processes that deliver optimized PPA," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "Through our strategic collaboration, we are enabling our customers to achieve next-generation HPC, mobile, 5G and AI designs and quickly launch their product innovations to the market."

The digital design flow, anchored by the tightly integrated Synopsys Fusion Design Platform™, features new technologies to ensure faster timing closure, full-flow correlation from synthesis to place-and-route to timing, as well as physical signoff. The platform has been enhanced to deliver improved synthesis and global placer engines that optimize library cell selection and placement results. To support TSMC's ultra-low-voltage design closure, the Synopsys optimization engine has been improved to use new footprint optimization algorithms. These new technologies, which result from the strategic partnership between the companies, will help provide a PPA boost for designs on TSMC's N3 process.

The Custom Compiler™ design and layout solution, part of the Synopsys Custom Design Platform, delivers improved productivity to designers using TSMC advanced process technologies. Numerous enhancements to Custom Compiler, validated by early 3nm users including the Synopsys DesignWare® IP team, reduce the effort to meet 3nm technology requirements. The Synopsys PrimeSim™ HSPICE®, PrimeSim SPICE, PrimeSim Pro and PrimeSim XA simulators, as part of the PrimeSim Continuum solution, deliver improved turnaround time for TSMC 3nm designs and provide signoff coverage for circuit simulation and reliability requirements.

"Our continued early collaboration with TSMC results in highly differentiated solutions for TSMC's advanced 3nm process technology that will provide customers designing complex SoCs with greater confidence of achieving successful outcomes," said Shankar Krishnamoorthy, general manager and corporate staff for the Silicon Realization Group at Synopsys. "With numerous technology innovations across the whole flow to enable 3nm, designers can take full advantage of the significant PPA improvements for their next-generation HPC, mobile, 5G and AI designs."

The following key products in the Synopsys design platforms have been enhanced to meet process requirements:

Digital Design Solutions

- Fusion Compiler™ RTL-to-GDSII solution
- Design Compiler® NXT synthesis solution
- IC Compiler II™ place-and-route solution

Signoff

- PrimeTime® timing signoff solution
- PrimePower power analysis

- StarRC™ parasitic extraction signoff
- IC Validator™ physical verification solution
- Tweaker™ ECO closure solution
- NanoTime custom timing signoff
- ESP-CV custom functional verification
- QuickCap® NX parasitic extraction 3D field solver

SPICE Simulation and Custom Design

- PrimeSim HSPICE, PrimeSim SPICE and PrimeSim Pro simulation solutions
- PrimeSim XA reliability analysis
- Custom Compiler custom design

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at https://www.synopsys.com.

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