Synopsys Accelerates Multi-Die Designs with Industry's First Complete HBM3 IP and Verification Solutions

HBM3 IP Solution Delivers Maximum Memory Bandwidth of 921 GB/s for High-Performance Computing, AI, and Graphics SoCs

MOUNTAIN VIEW, Calif., Oct. 7, 2021 /PRNewswire/ --

Highlights of this Announcement:

- The DesignWare HBM3 Controller, PHY, and Verification IP reduces integration risk and maximizes memory performance in 2.5D multi-die systems
- Low-latency HBM3 Controller with flexible configuration options enhance memory bandwidth
- Pre-hardened or configurable HBM3 PHY in 5-nm process operates at 7200 Mbps for up to 2X the data rate and improves power efficiency by up to 60% compared to HBM2E
- Verification IP and memory models for ZeBu and HAPS offer an end-to-end solution for rapid verification closure from IP to SoC
- Synopsys' 3DIC Compiler, an integrated multi-die design and analysis platform, provides a comprehensive HBM3 auto-routing solution for rapid and robust design development

Synopsys, Inc. (Nasdaq: SNPS) today announced the industry's first complete HBM3 IP solution, including controller, PHY, and verification IP for 2.5D multi-die package systems. HBM3 technology helps designers meet essential high-bandwidth and low-power memory requirements for system-on-chip (SoC) designs targeting high-performance computing, AI and graphics applications. Synopsys' DesignWare® HBM3 Controller and PHY IP, built on silicon-proven HBM2E IP, leverage Synopsys' interposer expertise to provide a low-risk solution that enables high memory bandwidth at up to 921 GB/s.

The Synopsys verification solution, including Verification IP with built-in coverage and verification plans, off-the-shelf HBM3 memory models for ZeBu® emulation, and HAPS® prototyping system, accelerates verification from HBM3 IP to SoCs. To accelerate development of HBM3 system designs, Synopsys' 3DIC Compiler multi-die design platform provides a fully integrated architectural exploration, implementation and system-level analysis solution.

Synopsys' DesignWare HBM3 Controller IP supports a variety of HBM3-based systems with flexible configuration options. The controller minimizes latency and optimizes data integrity with advanced RAS features that include error correction code, refresh management and parity.

The DesignWare HBM3 PHY IP in 5-nm process, available as pre-hardened or customer configurable PHY, operates at up to 7200 Mbps per pin, significantly improves power efficiency and supports up to four active operating states enabling dynamic frequency scaling. The DesignWare HBM3 PHY utilizes an optimized micro bump array to help minimize area. The support for interposer trace lengths gives designers more flexibility in the PHY placement without impacting performance.

Synopsys Verification IP for HBM3 uses next-generation native SystemVerilog Universal Verification Methodology architecture to ease integration of existing verification environments and run a greater number of tests, accelerating time to first test. The off-the-shelf HBM3 memory models for ZeBu emulation and HAPS prototyping system enable RTL and software verification for higher levels of performance.

"Synopsys continues to address the design and verification requirements of data-intensive SoCs with high-quality memory interface IP and verification solutions for the most advanced protocols like HBM3, DDR5 and LPDDR5," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "The complete HBM3 IP and verification solutions enable designers to meet increasing bandwidth, latency and power requirements while accelerating verification closure, all from a single, trusted provider."

Synopsys' broad DesignWare IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Our extensive investment in IP quality and comprehensive technical support enable designers to reduce integration risk and accelerate time-to-market. For more information, please visit https://www.synopsys.com/designware.

Supporting Customer and Partner Quotes

"Micron is committed to empowering the world's most advanced computing systems with the industry's highest performing solutions. HBM3 will deliver the memory bandwidth critical to enabling the next generation of high-performance computing and

artificial intelligence systems," said Mark Montierth, Micron vice president and general manager of High-Performance Memory and Networking. "Our collaboration with Synopsys will accelerate ecosystem development for ultra-high bandwidth, energy-efficient HBM3 products with unprecedented performance."

"The data driven era of computing and evolution of AI, HPC, graphics, and other applications have increased memory bandwidth requirements exponentially," said Kwangil Park, senior vice president of Memory Product Planning at Samsung Electronics. "As the world's leading memory chip maker, Samsung is continually focused on supporting ecosystem readiness and developing HBM to satisfy the growing bandwidth requirements across all applications. Synopsys is an ecosystem pioneer in the HBM industry and a valued partner. We look forward to continuing to provide the best HBM performance to our customers."

"SK hynix, a leading global semiconductor manufacturer, continues to invest in developing next-generation memory technologies, including HBM3 DRAMs, to meet the exponential growth in workloads for AI and graphics applications," said Cheol Kyu Park, vice president, HBM Product Champion and Head of DRAM Product Engineering at SK hynix. "We will leverage our long-standing relationship with Synopsys to provide our mutual customers with fully-tested and interoperable HBM3 solutions that can maximize memory performance, capacity and throughput."

"Socionext, a global leader in SoC solutions, together with Synopsys, an industry-leading partner, provide comprehensive solutions to our customers across a wide range of markets," said Yutaka Hayashi, vice president of Data Center & Networking Business Unit at Socionext. "Our recent collaboration with Synopsys, leveraging Synopsys' HBM2E IP on 5-nm process and integrated full-system multi-die design platform, will extend to include the new DesignWare HBM3 IP and verification solutions. As a result, our customers can achieve higher memory performance and capacity in SoCs requiring the upcoming HBM3 specification."

Availability and Resources

The Synopsys DesignWare HBM3 Controller, PHY, and Verification IP as well as the ZeBu emulation memory model, HAPS prototyping system, and 3DIC Compiler are available now.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

SOURCE Synopsys, Inc.