Synopsys Advances Processor IP Leadership with New ARC DSP IP Solutions for Low-Power Embedded SoCs

New ARC VPX DSPs Reduce Power and Area Up to Two-Thirds for IoT, AI, Automotive and Voice/Language Processing Designs

MOUNTAIN VIEW, Calif., Sept. 20, 2021 /PRNewswire/ --

Highlights of this Announcement:

- Synopsys ARC 128-bit VPX2 and 256-bit VPX3 DSP IP are based on same advanced VLIW/SIMD architecture as higher performance 512-bit VPX5, providing greater flexibility for specific application requirements
- Portfolio includes safety-enhanced implementations that meet random fault detection and systematic functional safety development flow requirements for full ISO 26262 compliance up to ASIL D
- MetaWare Development Toolkit with C/C++ compiler and associated libraries supports vector length-agnostic programming to accelerate code development and portability
- Attend the ARC Processor Virtual Summit on September 21 – 22, 2021, to learn more about the new ARC VPX DSPs and hear about the latest technologies and trends in processor IP

To address the broader range of power, performance and area (PPA) demands of embedded applications, Synopsys, Inc. (Nasdaq: SNPS) today announced it has expanded its DesignWare® ARC® Processor IP portfolio with new 128-bit ARC VPX2 and 256-bit ARC VPX3 DSP Processors. Based on the same VLIW/SIMD architecture as the company's higher performance 512-bit ARC VPX5 DSP processor, the new additions deliver up to two-thirds lower power and area. The ARC VPX DSP IP family now provides greater flexibility for designers to optimize their designs based on the unique power, performance and area (PPA) requirements of embedded workloads such as IoT sensor fusion, radar and LiDAR processing, engine control, voice/speech recognition, natural language processing and other edge AI applications.

"AI-enabled devices have an increasing need for specialized processors that can handle a variety of DSP and machine learning workloads with a high degree of energy efficiency," said CL Chen, COO at Neuchips, a leading AI domain specific compute solutions startup in Taiwan. "By expanding the ARC VPX processor family to support a range of vector lengths, Synopsys enables designers targeting a broader set of applications to implement high-performance signal processing in their designs."

"By expanding the ARC DSP processor portfolio with support for smaller vectors, Synopsys is enabling signal processing and AI in size, power, and thermally-constrained systems," said Jim McGregor, Principal Analyst at Tirias Research. "In addition, the ultra-high floating-point performance and functional safety compliance of the VPX processors make them especially well-suited for the growing number of IoT applications like automotive, medical systems, and industrial automation. Synopsys' ARC processors have been used by over 250 customers worldwide who collectively ship more than 2.5 billion ARC-based chips annually."

Scalable and Highly Configurable DSP Processors

The smaller vector-length ARC VPX2 and VPX3 DSP processors, optimized for highly parallel processing with minimal energy and area consumption, are available in single- or dual-core configurations to address a broad range of application requirements. Each VPX core contains a scalar execution unit and multiple vector units that support 8-bit, 16-bit and 32-bit SIMD computations. The VPX DSPs support half-, single-, and double-precision floating point formats, and up to three floating point pipelines are available in each VPX core. The unique hardware acceleration for special math functions used in linear and non-linear algebra functions deliver high-precision results. The new VPX DSPs include enhancements to the instruction set architecture (ISA) and load/store bandwidth to deliver up to twice the performance of existing offerings for common DSP functions such as fast Fourier transforms (FFTs). In addition, the safety-enhanced ARC VPX2FS and VPX3FS integrate hardware safety features including error correction code (ECC) protection for memories and interfaces, safety monitors and lockstep mechanisms that help designers achieve the most stringent levels of ISO 26262 ASIL B, ASIL C and ASIL D functional safety compliance.

Comprehensive Software Development Environment

Like all Synopsys ARC processors, the VPX2 and VPX3 processors are supported by the Synopsys ARC MetaWare Development Toolkit, which provides a vector length-agnostic software programming model specifically optimized for the VPX hardware architecture. The MetaWare compiler's auto-vectorization feature transforms sequential code into vector operations for maximum throughput. Together with a robust set of software libraries that include DSP, machine learning and linear algebra functions, the MetaWare Development Toolkit delivers a comprehensive programming environment that accelerates time to

optimum results and simplifies software portability.

"We continue to build on our industry leadership by expanding the DesignWare ARC processor family with the latest VPX DSP processors," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "Synopsys provides designers with a full range of scalable, software-compatible DSP IP solutions that address the varying performance, power and area requirements across a chip family."

The broad Synopsys DesignWare IP portfolio includes logic libraries, embedded memories, IOs, PVT monitors, embedded test, analog IP, interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, the company's IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality and comprehensive technical support enable designers to reduce integration risk and accelerate time-to-market. For more information, please visit https://www.synopsys.com/designware.

Availability

- The Synopsys DesignWare ARC VPX2 and VPX3 DSP Processor IP is scheduled to be available to lead customers in calendar Q4 2021.
- The Synopsys DesignWare ARC VPX2FS and VPX3FS Processor IP is scheduled to be available to lead customers in calendar Q1 2022.

Additional information can be found here.

ARC Processor Virtual Summit, Sept 21-22, 2021

The ARC Processor Virtual Summit will deliver all the practical knowledge you need to meet your unique PPA requirements. The summit includes a special keynote, TinyML and Efficient Deep Learning from Song Han, assistant professor of EECS at MIT. Han will teach TinyML techniques to help you address artificial intelligence's (AI's) extraordinary requirements for data, computation, and power in a way that will make your designs greener, faster, more efficient, and sustainable. Register to attend the event.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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