Synopsys Strategic Partnership with Samsung Foundry Accelerates Access to Transformative 3nm GAA Technology

Fusion Design Platform Advancements Provide New Levels of Power-Optimized Performance for High-Growth AI, HPC and 5G Markets

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Highlights for this Announcement:

- Gate-all-around (GAA) transistor architecture offers new opportunities and degrees of freedom to meet the exacting demands of power- and performance-sensitive designs
- Collaborative R&D pathfinding delivers critical innovations in GAA-focused power-optimization techniques, enabling leading PPA entitlement and achievement of maximum performance-per-Watt
- Successful tapeout of a complex, multi-subsystem SoC leads to the accelerated qualification of Synopsys Fusion Design Platform for Samsung Foundry's latest 3nm GAA process technology

Synopsys, Inc. (Nasdaq: SNPS) today announced that the Synopsys Fusion Design Platform™ has enabled Samsung Foundry to achieve first-pass silicon success for an advanced, high-performance and multi-subsystem system-on-chip (SoC), validating the extended power, performance and area (PPA) benefits of its next-generation, 3-nanometer (nm) gate-all-around (GAA) process technology. This tapeout is the culmination of an extensive collaboration between Synopsys and Samsung Foundry to accelerate the delivery of a highly optimized reference methodology that realizes the maximum power and performance opportunities inherent to the latest 3D transistor architecture.

The reference flow from Synopsys deploys the full breadth of Synopsys' highly integrated Fusion Design Platform, including the industry's only integrated and golden-signoff-enabled RTL-to-GDSII design flow coupled with the most trusted, golden-signoff products. Customers targeting Samsung Foundry's latest 3-nm GAA process can realize the maximum PPA entitlement for next-generation designs spanning high-performance computing (HPC), 5G, mobile and advanced, artificial intelligence (AI) applications.

"Samsung Foundry is at the heart of fueling the next phase of industry innovation with our continued process-technology-based evolutions to meet the growing demands of both specialized and broad-market applications," said Sangyun Kim, Vice President of Foundry Design Technology Team at Samsung Electronics. "Our latest, advanced 3nm GAA process has benefited from our extensive collaboration with Synopsys, and the accelerated readiness of the Fusion Design Platform to enable the efficient realization of the 3nm process' promise, is a testament to the importance and benefit of these key alliances."

The GAA architecture delivers a tapeout-proven path to higher transistor densities through continued, Moore-centric area scaling. Inherent to the GAA architecture are improved electrostatic properties that translate to increased performance and reduced power with the added benefit of new optimization opportunities based on the additional vector of nano-sheet-width control. Allied to well-established voltage-threshold tuning, this extra degree of freedom expands the optimization solution space enabling much more refined control in realizing overarching target-design PPA metrics. Synopsys and Samsung have shared an extensive collaboration in accelerating the availability and maximizing the benefits for this watershed technology, resulting in full-flow, highly convergent optimization advancements in Synopsys' Fusion Compiler™ and IC Compiler™ II.

Additional advanced-node challenges, including support for complex placement methodologies and floorplan rules, new routing rules and increased variability, have been seamlessly addressed through product advancements spanning the Synopsys Fusion Design Platform. Based on a single data model and sharing a common optimization architecture, the platform ensures single-point technology enablement that delivers optimized design convergence, maximum systemic margin elimination, and the fastest time to closure.

"The GAA transistor structure marks a key inflection point in process-technology advancement that is critical in maintaining the scaling trajectories needed for the next wave of hyperscale innovation," said Shankar Krishnamoorthy, general manager of the Digital Design Group at Synopsys. "Our strategic collaborations with Samsung Foundry in support of the co-delivery of best-in-class technologies and solutions are ensuring the continuation of these scaling trends and the associated opportunities these offer to the broader semiconductor industry."

Synopsys technology files are available from Samsung Foundry for the 3nm GAA technology process. Key products in the Synopsys Fusion Design Platform that are qualified include:

Digital design

- Fusion Compiler, the industry's only RTL-to-GDSII product
- IC Compiler II place-and-route solution
- Design Compiler® RTL-synthesis solution

Signoff

- PrimeTime® industry's gold-standard timing-signoff solution
- StarRC™ extraction-signoff solution
- IC Validator ™ physical-signoff solution
- SiliconSmart® library-characterization solution

For more information about fully qualified flow features from Synopsys that are optimized for Samsung Foundry 3nm GAA process technologies, visit www.synopsys.com/fusion.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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