

Synopsys Expands Multi-Die Solution Leadership with Industry's Lowest Latency Die-to-Die Controller IP

Complete DesignWare Die-to-Die Controller and PHY IP Solution Maximizes Performance for Efficient Inter-Die Connectivity in High-Performance Computing, AI and Networking SoCs

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Highlights of this Announcement:

- The complete DesignWare Die-to-Die IP solution, including controller, 112G USR/XSR and HBI PHYs, supports die splitting and compute scaling
- New Die-to-Die Controller's error correction mechanisms with replay and optional forward error correction minimize bit error rate for reliable die-to-die links
- Low-latency architecture supports AMBA CXS for efficient interface with Arm® Neoverse™ Coherent Mesh Network
- Synopsys provides a complete multi-die solution with Die-to-Die IP, HBM IP and 3DIC Compiler for system-in-package integration

Synopsys, Inc. (Nasdaq: [SNPS](#)) today announced its new [DesignWare® Die-to-Die Controller IP](#), which complements the company's existing 112G USR/XSR PHY IP for a complete die-to-die IP solution. With the complete IP solution, designers benefit from a low-latency, high-bandwidth die-to-die connectivity offering that addresses the increased workload and faster data movement demands of high-performance computing, artificial intelligence (AI) and networking SoCs. The DesignWare Die-to-Die Controller and PHY IP are part of the Synopsys multi-die solution, consisting of HBM IP and 3DIC Compiler, accelerating SoC designs requiring advanced packaging.

"Interconnect technology is increasingly vital for the next-generation of performant, customized infrastructure SoCs," said Jeff Defilippi, director of product management, Infrastructure Line of Business, Arm. "With its low-latency, native support for AMBA CXS, Synopsys DesignWare Die-to-Die Controller can easily integrate with the Arm Coherent Mesh Network to provide our mutual customers access to the multichip IP solutions offering new scale-up performance and composability options required for this next era of infrastructure compute."

The DesignWare Die-to-Die Controller provides error recovery mechanisms such as optional forward-error correction and cyclic redundancy check for higher data integrity and link reliability. The DesignWare Die-to-Die controller's flexible configuration supporting the AMBA® CXS and AXI protocols allows coherent and non-coherent data communication for easy integration into Arm-based and other high-performance SoCs. The DesignWare Die-to-Die Controller with support for up to 1.8Tb/s PHY bandwidth addresses high-performance computing demands of SoCs requiring robust die-to-die connectivity.

"The trend of die splitting and disaggregation require ultra- and extra-short reach links to enable inter-die connectivity with high data rates," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "Our complete DesignWare Die-to-Die IP solution offers ultra-low-latency controller and high-performance PHYs that have been adopted by multiple customers, allowing designers to integrate high-quality IP in their multi-die SoCs with confidence while minimizing integration risk."

Synopsys' broad DesignWare IP portfolio includes logic libraries, embedded memories, IOs, PVT monitors, embedded test, analog IP, interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative

offers IP prototyping kits, IP software development kits and IP subsystems. Our extensive investment in IP quality and comprehensive technical support enable designers to reduce integration risk and accelerate time-to-market. For more information, please visit <https://www.synopsys.com/designware>.

Availability and Resources

The DesignWare Die-to-Die Controller IP is available now to early adopters. The Synopsys DesignWare Die-to-Die USR/XSR PHY IP in 12nm, 7nm and 5nm processes are available now with a roadmap to 3nm. The HBI PHY IP in 7nm and 5nm processes are available now.

For more information, visit the [DesignWare Die-to-Die IP](#) page.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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