Synopsys DesignWare PVT Subsystem Drives Performance, Power and Silicon Lifecycle Management on TSMC's N3 Process Technology

Real-Time Chip Insights Provide Optimized Device Utilization Throughout the Silicon Lifecycle for Leading Market Applications

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Highlights for this Announcement:

- DesignWare PVT monitoring and sensing subsystem IP supports cutting-edge technologies targeting AI, data center, HPC, consumer and 5G markets
- Innovative, modular architecture offers new sensor technologies for advanced node devices
- Designers benefit from a complete PVT subsystem providing real-time insights within the chip

Synopsys, Inc. (Nasdaq: SNPS) today announced the availability of its DesignWare® process, voltage and temperature (PVT) monitoring and sensing subsystem IP on TSMC's industry-leading N3 process technology. The PVT monitoring and sensing subsystem IP has been added to the TSMC9000 Program, TSMC library and IP quality management program, offering customers a highly competitive performance advantage for a wide variety of target market applications including artificial intelligence (AI), data center, high-performance computing (HPC), consumer and 5G. SoC designers targeting TSMC's most advanced process can utilize the deeply embedded PVT monitoring and sensing subsystem technology to assess key chip parameters during production as well as for measurement and analysis of real-time dynamic conditions during every stage of the device life cycle.

In-chip sensing from Moortec, which is now a part of Synopsys, continues to be an essential element to achieve the highest levels of performance and reliability within today's advanced process technologies, underpinning optimization schemes, telemetry, and analytics. The IP within the subsystem is a foundational element of Synopsys' Silicon Lifecycle Management (SLM) platform. The SLM process begins with the placement of the in-chip sensors and PVT monitors deep within the chip. The data they provide facilitates a greater understanding of chip performance and power activity and enables the SLM platform's analytics engines to drive more detailed and precise optimizations at each stage of the semiconductor lifecycle, from the early design phase, through in-field mission mode operation.

"TSMC continues to work with our ecosystem partners to address customers' design challenges in power and performance and enable next-generation silicon innovation with design solutions using TSMC's latest technologies," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "The new Synopsys DesignWare PVT monitoring IP is a demonstration of the value of our ongoing collaboration with Synopsys and will allow continued product support for our mutual customers as they benefit from the power and performance advantages of TSMC's N3 process technology."

The innovative, modular design of the DesignWare PVT subsystem offers a fabric of PVT monitors that are highly configurable based on the target application. This latest solution for TSMC N3 process technology includes a distributed thermal sensor enabling highly localized thermal analysis, a new catastrophic trip sensor for programmable protection against thermal runaway and an additional thermal diode providing an independent measure of die temperature even when the chip is powered off. The whole system is controlled by a fourth-generation PVT controller which allows easy access to data from multiple instantiations of the individual embedded monitors and sensors.

"Driven by the demand for ever-increasing design complexity and device gate density, the adoption of PVT monitoring is now critical to successful advanced node chip design," said Amit Sanghani, vice president of Hardware Analytics and Test Group at Synopsys. "The full suite of DesignWare embedded PVT monitors and sensors, part of Synopsys' innovative new Silicon Lifecycle Management Platform, will offer the design community innovative in-chip sensing technologies, real-time deep chip insights, and enhanced product utilization throughout the silicon lifecycle."

The DesignWare PVT monitoring and sensing subsystem can be configured to specific sector applications and is now available for early customer integration. For more information, visit DesignWare in-chip PVT monitoring and sensing IP.

About Synopsys DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on Synopsys DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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