Arm Leverages Synopsys Fusion Compiler to Enable Best PPA for Latest Neoverse Platforms

Architecturally Targeted Optimizations Accelerate the Development of Arm Neoverse V1 and N2 Platforms; Deliver Best-In-Class Performance-Per-Watt

MOUNTAIN VIEW, Calif., April 28, 2021 /PRNewswire/ --

Highlights of this Announcement:

- Synopsys' Fusion Compiler RTL-to-GDSII solution's unique, single data model-based infrastructure coupled with a single-shell, hyper-converged optimization architecture unlocks optimal PPA potential for advanced Arm-based CPU cores
- Tightly integrated synthesis within Fusion Compiler delivers full-flow correlated design exploration, helping designers quickly converge to their optimal SoC architecture
- Unmatched design capacity and throughput, coupled to advanced hierarchical methodologies, accelerate big-core development time, hastening time-to-market

Synopsys, Inc. (Nasdaq: SNPS) today announced that Fusion Compiler™, the industry's only single data model and golden signoff-enabled RTL-to-GDSII implementation solution, has been deployed by Arm to enable optimal power, performance and area (PPA) on next-generation Arm® Neoverse™ V1 and N2 infrastructure cores. The latest advances in the Fusion Compiler solution extend the unique benefits of its single-shell, hyper-convergent optimization architecture, enabling designers to extract the maximum performance per watt on their Arm Neoverse-based system-on-chip (SoC) designs targeting broad-market applications including data center infrastructure, high-performance computing, 5G and AI. The Synopsys and Arm reference methodology is immediately available through QuickStart Implementation Kits for these new cores providing an accelerated path to design closure and bring-up.

"Hyperscale computing and cloud workloads demand a scalable, performance-per-watt optimized architecture, and the new Arm Neoverse platforms comprehensively answer that demand," said Jeff Kehl, vice president of CPU Engineering, Central Engineering at Arm. "Our collaboration with Synopsys and the deployment of Fusion Compiler delivers accelerated access to this highly optimized technology, enabling our mutual customers to design and deploy market-shaping solutions into the fast-expanding hyperscale space."

Synopsys' Fusion Compiler RTL-to-GDSII solution is uniquely architected to enable design teams to achieve the optimal levels of PPA in the most convergent manner to ensure the fastest and most predictable time-to-results. It utilizes a highly scalable, unified data model and comprises an analysis backbone that leverages technology from the industry's golden-signoff analysis tools, all within a single, integrated shell, enabling unique customized flows for best quality of results (QoR) and signoff correlation. The Fusion Compiler solution's interleaved optimization engines ensure that critical PPA metrics are optimized efficiently and effectively throughout the full implementation flow. Additionally, its unique architecture is augmented by "machine learning everywhere" technologies, enabling new levels of productivity and QoR.

"Synopsys and Arm share a long-standing partnership with the common goal of continuing to raise the bar and push the envelope for lowest-power, high-performance computing," said Shankar Krishnamoorthy, general manager of Digital Design Group at Synopsys. "Arm's application of Total-Compute principles across their entire IP portfolio shares many parallels with Synopsys' total-integration focus for the Fusion Design Platform, both having the goal of delivering the best end-to-end results and design experience. This successful collaboration has comprehensively delivered on our shared goal by enabling Fusion Compiler to achieve new levels of PPA for the Neoverse V1 and N2 cores."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454

simone@synopsys.com

SOURCE Synopsys, Inc.