Synopsys Launches Industry's First Complete IP Solution for PCI Express 6.0

DesignWare IP for PCI Express 6.0 Delivers 64 GT/s Data Rate with Low Latency for High-Performance Computing, AI and Storage SoCs

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Highlights:

- DesignWare Controller, PHY and Verification IP supports the latest features in the PCI Express 6.0 specification, enabling early SoC development
- Low-latency controller with new MultiStream architecture delivers up to 2X the throughput of a conventional PCI Express controller
- High-performance PHY in 5-nm process with unique analog and DSP techniques provides 20 percent less power across chip-to-chip, riser card and backplane interfaces
- Comprehensive set of protocol, methodology and productivity features enable rapid verification of PCI Express 6.0 designs

Synopsys, Inc. (Nasdaq: SNPS) today announced the industry's first complete IP solution for the PCI Express® (PCIe®) 6.0 technology that includes controller, PHY and verification IP, enabling early development of PCIe 6.0 system-on-chip (SoC) designs. Built on Synopsys' widely deployed and silicon-proven DesignWare® IP for PCIe 5.0, the new DesignWare IP for PCIe 6.0 supports the latest features in the standard specification including, 64 GT/s PAM-4 signaling, FLIT mode and L0p power state. Synopsys' complete IP solution addresses evolving latency, bandwidth and power-efficiency requirements of high-performance computing, AI and storage SoCs.

To achieve the lowest latency with maximum throughput for all transfer sizes, the DesignWare Controller for PCI Express 6.0 utilizes a MultiStream architecture, delivering up to 2X the performance of a single-stream design. The Controller, with available 1024-bit architecture, allows designers to achieve 64 GT/s x16 bandwidth while closing timing at 1GHz. In addition, the controller provides optimal flow with multiple data sources and in multi-virtual channel implementations. To facilitate accelerated testbench development with built-in verification plan, sequences and functional coverage, the VC Verification IP for PCIe uses native SystemVerilog/UVM architecture that can be integrated, configured and customized with minimal effort.

Synopsys' DesignWare PHY IP for PCIe 6.0 provides unique adaptive DSP algorithms that optimize analog and digital equalization to maximize power efficiency regardless of the channel. The PHY enables near zero link downtime using patent-pending diagnostic features. The placement-aware architecture of the DesignWare PHY IP for PCIe 6.0 minimizes package crosstalk and allows dense SoC integration for x16 links. The optimized datapath with ADC-based architecture achieves ultra-low latency.

"Advanced cloud computing, storage and machine learning applications are transferring significant amounts of data, requiring designers to incorporate the latest high-speed interfaces with minimal latency to meet the bandwidth demands of these systems," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "With Synopsys' complete DesignWare IP solution for PCI Express 6.0, companies can get an early start on their PCIe 6.0-based designs and leverage Synopsys' proven expertise and established leadership in PCI Express to accelerate their path to silicon success."

"PCI Express is the most widely-adopted and extensible interconnect technology in history," said Jim Pappas, director of Technology Initiatives at Intel. "Synopsys' latest DesignWare IP for PCIe 6.0 is a leading indicator of the global ecosystems' ongoing commitment to this important industry standard and sets the stage for PCIe Gen 6 development and adoption on future Intel platforms."

Availability and Resources
The DesignWare Controller and PHY IP for PCIe 6.0 early access are scheduled to be available in Q3 of 2021. The Verification IP for PCIe 6.0 is available now. For more information, visit DesignWare IP for PCIe 6.0.

About Synopsys DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers

to reduce integration risk and accelerate time-to-market. For more information on Synopsys DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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