Synopsys Announces Euclide to Accelerate Design and Verification Productivity

Finds Bugs Early and Optimizes Code for Design Compiler, VCS and ZeBu

MOUNTAIN VIEW, Calif., March 3, 2021 /PRNewswire/ --

Highlights:

- Interactive and incremental analysis enables early detection of design bugs
- Correct-by-construction coding ensures RTL compatibility for Design Compiler and ZeBu
- Real-time checks help to avoid costly testbench errors and increase VCS performance
- Integration with Verdi for seamless debug and code development
- Built-in SystemVerilog/UVM compliance assures best coding practices across verification teams

Synopsys, Inc. (Nasdaq: SNPS) today introduced Synopsys Euclide, the industry's next-generation hardware description language (HDL)-aware integrated development environment (IDE). Synopsys Euclide enables engineers to find bugs earlier and optimize code for design and verification flows by identifying complex design and testbench compliance checks during SystemVerilog and Universal Verification Methodology (UVM) development.

Euclide accelerates correct-by-construction code development through context specific autocompletion and content assistance that is tuned for Synopsys VCS® simulation, Verdi® debug, ZeBu® emulation, and compatible with Design Compiler® NXT synthesis solutions, helping engineers to improve code quality during the entire project development cycle.

"The on-the-fly design and testbench checks in Synopsys Euclide have helped us in unmasking critical bugs otherwise identified at late design stages," said Assaf Shacham, Senior Hardware Engineering Manager at Microsoft Corporation. "In addition, the efficiency of our experienced design and verification engineers, as well as the learning curve of new engineers has significantly improved by using the various IDE coding acceleration and code exploration features."

Ever-increasing system-on-chip complexity requires robust and error-free design and testbench code. The advanced algorithms in Synopsys Euclide enable running high performance compilation, elaboration and pseudo-synthesis that provide real-time feedback to improve design and testbench quality at the time of code development. The innovative engine architecture allows incremental analysis, error recoverability and produces advanced feedback on incomplete code. Identifying bugs early helps to avoid unnecessary simulation cycles, lengthy debug sessions and chip re-spins.

"Synopsys Euclide is a unique, innovative and highly interactive code development platform that accelerates design and testbench development for VCS users." said Sandeep Mehrotra, vice president of engineering in the Verification Group at Synopsys. "With Euclide, engineers can detect bugs early, ensure RTL code compatibility with Design Compiler and ZeBu, and optimize simulation performance with VCS."

Availability and Resources

The Synopsys Euclide on-the-fly code checking solution is available now. VCS andVerdi users can easily adopt the solution using existing project files and scripts. For more information, visit Euclide Integrated Development Environment.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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