Synopsys Demonstrates Silicon Proof of DesignWare 112G Ethernet PHY IP in 5nm Process for High-Performance Computing SoCs

DesignWare IP With Unmatched Long-Reach Performance Results Supports Insertion Loss Greater Than 40dB and Delivers Power-Efficiency of Less Than five pJ/Bit

MOUNTAIN VIEW, Calif., Jan. 28, 2021 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced the silicon proof of DesignWare® 112G Ethernet PHY IP in 5nm FinFET process, delivering significant performance, power and area advantages. The area-efficient DesignWare 112G Ethernet PHY enables designers to optimize highly dense system-on-chips (SoCs) with placement-aware IP that maximizes bandwidth per die-edge through stacking and placement on all four edges of the die. To extend performance, the DesignWare 112G PHY demonstrates zero bit-error rate post forward-error correction in greater than 40dB channels while offering power-efficiency of less than five picojoules per bit (pJ/bit).

Combined with Synopsys' routing feasibility study, packages substrate guidelines, signal and power integrity models, and thorough crosstalk analysis, Synopsys provides a comprehensive 112G Ethernet PHY solution for fast, reliable SoC integration. DesignWare 112G Ethernet PHY is an integral part of Synopsys' comprehensive IP portfolio for high-performance cloud computing applications, including widely used protocols such as PCI Express®, DDR, HBM, Die-to-Die, CXL and CCIX.

"As the industry's trusted IP provider for over two decades, designers rely on Synopsys to deliver feature-rich, high-speed SerDes IP in the most advanced processes to help them gain a competitive advantage in the market," said John Koeter, senior vice president of marketing and strategy for IP at Synopsys. "The comprehensive DesignWare 112G Ethernet PHY IP solution in 5nm FinFET process with differentiated performance, power and area enables designers to significantly reduce their integration risk for a faster path to silicon success."

Additional Resources

For more information, visit DesignWare 112G Ethernet PHY IP.

About DesignWare IP

Synopsys is a provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As an S&P 500 company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and offers the industry's broadest portfolio of application security testing tools and services. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing more secure, high-quality code, Synopsys has the solutions needed to deliver innovative products. Learn more at www.synopsys.com.

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