Breakthrough Synopsys IC Validator Technologies Deliver Faster Physical Signoff Convergence

New Elastic CPU, Explorer LVS, and Machine Learning Features Deliver Accelerated Time-to-Results for Automotive, High-Performance Computing, AI, Networking and Wireless Applications

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Highlights:

- Industry's first elastic CPU management technology delivers 40 percent lower cost of ownership for physical verification signoff
- Machine-learning driven root cause analysis enables faster design convergence
- Innovative Explorer layout versus schematic (LVS) delivers 30X faster LVS with 30X smaller memory during SoC integration

Synopsys, Inc. (Nasdaq: SNPS) today announced the immediate availability of the latest release of its IC Validator physical verification solution, which includes several new innovative technologies to accelerate time-to-results for leading-edge applications. IC Validator's unique elastic CPU management technology delivers up to 40 percent compute savings in physical signoff for both on-premise and cloud environments. Another new technology in IC Validator includes machine-learning driven root cause analysis that automatically identifies critical design rule checking (DRC) issues enabling faster DRC closure. Additionally, the Explorer layout versus schematic (LVS) technology offers up to 30X faster runtime and order of magnitude debugging speed-up during SoC integration.

"Customers developing leading-edge designs continually face design-closure challenges due to growing design sizes and manufacturing complexity. On-time physical verification closure is essential to meet demanding tapeout schedules," said Raja Tabet, senior vice president of Engineering, Design Group at Synopsys. "Our IC Validator's innovations will provide designers with faster performance, productivity, and a faster path to production silicon."

IC Validator, a key component of Synopsys' Fusion Design Platform™ and Custom Design Platform™, is a comprehensive and highly scalable physical verification solution that includes DRC, LVS, programmable electrical rule checks (PERC), dummy metal fill, and design-for-manufacturability (DFM) enhancement capabilities. Architected for high performance and scalability, IC Validator maximizes mainstream hardware utilization, using smart memory-aware load scheduling and balancing technologies. It uses both multi-threading and distributed processing across multiple machines to provide scalability benefits that extend to thousands of CPUs.

IC Validator verification in Synopsys' Fusion Design Platform enables fast DRC checking, automatic fixing, timing aware fill insertion and signoff accurate STAR RC™ integration to accelerate convergence. IC Validator's live DRC technology provides on-demand verification for immediate DRC feedback in Synopsys' Custom Design Platform.

Learn more about Synopsys IC Validator's new technologies at https://www.synopsys.com/implementation-and-signoff/physical-verification.html.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

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