Synopsys Collaborates with TSMC to Accelerate 3nm Innovation, Enabling Next-Generation SoC Design

Certified Synopsys design solutions enable HPC, mobile, 5G, and AI SoCs and offer cutting-edge power savings and performance

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Highlights:

- Requirements in growth semiconductor segments are driving the state-of-the-art in silicon process geometry
- Synopsys and TSMC have extensively collaborated on enablement of Synopsys full-flow digital and custom design platforms to unlock PPA benefits of TSMC's 3nm process technology while accelerating time to market
- Key Synopsys products have been further enhanced to support advanced requirements for TSMC N3 process

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified Synopsys' digital and custom design platforms for TSMC's 3-nanometer (nm) process technology. This certification, based on TSMC's latest design rule manual (DRM) and process design kits (PDKs), is the result of an extensive collaboration with rigorous validation to deliver design solutions for optimized power, performance, and area (PPA), which accelerate the path to next-generation designs.

"We're pleased with the result of our multi-year collaboration with Synopsys in delivering platform solutions on TSMC's advanced process that help our mutual customers achieve silicon innovations benefiting from the significant power and performance boost of our 3nm process technology and quickly launch their new product innovations to market," said Suk Lee, senior director of the Design Infrastructure Management Division at TSMC. "Certification of the Synopsys design solutions enables our mutual customers' designs to be implemented on TSMC N3 process with high confidence for optimized PPA."

Through a close collaboration with TSMC, Synopsys developed key enablement features and new technologies to ensure full-flow correlation from synthesis to place-and-route to timing and physical signoff for TSMC's N3 processes. Synopsys' Fusion Compiler™ RTL-to-GDSII solution and IC Compiler™ II place-and-route solution have been enabled with extended support of TSMC's N3 process. Synopsys' Design Compiler® NXT synthesis solution has been enhanced to enable designers to take full advantage of TSMC's 3nm technology, delivering improved quality of results (QoR) and tighter correlation to Synopsys' IC Compiler™ II place-and-route solution using a new, highly accurate approach to resistance and capacitance estimation. The PrimeTime® signoff solution supports the advanced multi-input switching (MIS) for accurate timing analysis and signoff closure. Additionally, Design Compiler NXT is enabled for TSMC N3 process for both HPC and mobile designs.

To optimize some of the special features with the TSMC 3nm process technology, the Synopsys digital design platform has been enhanced to support pin density aware placement and global route modeling for better routing convergence on standard cell pins, concurrent legalization and optimization (CLO) for faster timing convergence, a new cell map (cell density) infrastructure to maximize available white space to improve PPA, interconnect optimization by auto generating via pillar structures and partial parallel routing for HPC design, and power-aware mixed driving strength multi-bit flip flop optimization for low-power designs.

In the Synopsys custom design platform, Custom Compiler has been enhanced to accelerate the implementation of 3nm analog designs. These enhancements – co-developed with and validated by early 3nm users, including the Synopsys DesignWare® IP team – reduce the effort to meet new design rules and other 3nm technology requirements. The Synopsys HSPICE®, FineSim® and CustomSim™ simulation solutions deliver enhanced turnaround time for TSMC 3nm designs and provide signoff coverage for TSMC 3nm circuit simulation and reliability requirements.

"Our collaboration with TSMC on highly differentiated solutions for its advanced 3nm process technology allows customers to begin designing their increasingly complex SoCs with greater confidence," said Charles Matar, senior vice president of System Solutions and Ecosystem Enablement for the Design Group at Synopsys. "The result of our collaboration enables designers to take full advantage of the significant power, performance, and area improvements of an advanced EUV process, while accelerating the innovation for their differentiated SoCs."

Synopsys technology files are available from TSMC for the 3nm technology process. Key products in the

Synopsys design platforms are certified:

Digital design solutions

- Fusion Compiler and IC Compiler II place-and-route solutions

Signoff

- PrimeTime timing signoff
- PrimePower power signoff
- StarRC™ extraction signoff
- IC Validator physical signoff
- NanoTime custom timing signoff
- ESP-CV custom functional verification
- QuickCap® NX parasitic field solver

SPICE simulation and custom design

- HSPICE, CustomSim, and FineSim simulation solutions
- CustomSim reliability analysis
- Custom Compiler™ custom design

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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